AN IMPROVED MODELING TECHNIQUE FOR CMOS GATES

by

Divyesh Kumar Shah

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

March 2000

AN IMPROVED MODELING TECHNIQUE FOR CMOS GATES

a thesis submitted

in partial fulfilment of the requirements

for the degree of

Master of Technology

by

Divyesh Kumar Shah

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

March 2000

CERTIFICATE

It is certified that the work presented in this thesis entitled "AN IMPROVED MODELING TECHNIQUE FOR CMOS GATES" has been carried out by **Mr. Divyesh Kumar Shah** (Roll No. 9810418) under my supervision and has not been submitted elsewhere for a degree.

(Dr. S. Qureshi)
Professor
Department of Electrical Engineering
Indian Institute of Technology
Kanpur 208016

ABSTRACT

Design of circuits is carried out in a hierarchical manner with verification done through simulations at each level of the hierarchy The timing simulators are used for finding out the delay of the designed circuits at the electrical level Simulators like SPICE give very accurate information regarding the delays but they are not useful for simulating very large circuits as they consume lot of time Many simple models have been proposed to develop fast timing simulators but they have resulted in loss of accuracy owing to the simplified models that they use Research is going on to attain a considerably accurate as well as efficient models

One such model that has been proposed was studied and the reason for the loss of accuracy pointed out The complete modeling has been redone with suitable corrections applied and the gain in accuracy with a very minute loss in efficiency is demonstrated

Dedicated to

My Beloved Parents

&

My Late Grand Ma

ACKNOWLEDGEMENTS

I am greatly indebted to my Guide Dr S Qureshi for his support and help through out the project work It was only because of his extended co operation and the freedom of thought that he encouraged that a work of this magnitude could be accomplished The completely open and free atmosphere that I enjoyed doing my thesis under him is unparalleled

I also express my sincere thanks to my parents brother and bhabhi who by their unending moral support encouraged me through out my M Tech program I also express my thanks to all the faculty because of whom I could improve my knowledge during my academic program

I would like to thank all my friends who with their strong support and help encouraged me all the time The thesis would not have been in the present shape had it not been for their open help and support Especially I would like to thank Cheeku Raju Murthy and Tadi for their help in the thesis work I am also grateful to Chillar Universal Sudheer Swaroop, Ultimate PAV Boddu Tanga Metallic Kovvi Photo Guduru Gupta Shanku&Sudheer Proff et al for making my stay enjoyable at IIT

INDEX

LIST OF FIGURES

Chapter 1

Chapter 2

Chapter 3

LIST OF TABLES

Chapter 4

CHAPTER 1
INTRODUCTION

Design of circuits has become a complex task with the state of the art chips containing millions of transistors. Design of circuits is carried out in a hierarchial manner with the design first done at the behavioral level and then translated down to the final physical level step by step. Verification of the design is necessary so that the final chip functions properly. If this verification is carried out at the final physical level and is found not to match specifications, then once again the circuit needs to be designed at the behavioral level and all the intermediate steps need to be repeated once again. So to avoid this wastage of time and effort, verification is carried out at each step before being translated to the next level. This verification is carried out by using simulators.

With the complexity of circuits increasing day by day, the demand for a very fast yet effective and accurate simulation is increasing. The problem lies in that if the simulator is designed to be highly accurate, then due to the complexity of the models required for such a simulator, the speed of the simulation decreases. In order to reduce the time of simulation, if the models are simplified, they result in errors that become unacceptable. So many new techniques for this simulation have been proposed and developed to have an optimum simulator.

1.1 SIMULATION

To make the task of designing complex circuits easy, a hierarchial design and verification procedure is used. In this the overall task is partitioned into more manageable components using various levels of abstraction. The different levels of abstractions vary from each other by the size of the components and the accuracy of the models used to depict these components. This reduces the overall verification time required, because at the highest level (behavioral level) information about the internal structure is missing and only the high level functionality of the system needs to be

verified If the circuit is as per the specifications then it can be translated to the next level and now with some more details added a more detailed verification can be carried out The design and verification flow for any circuit will be as shown in Figure 1 1

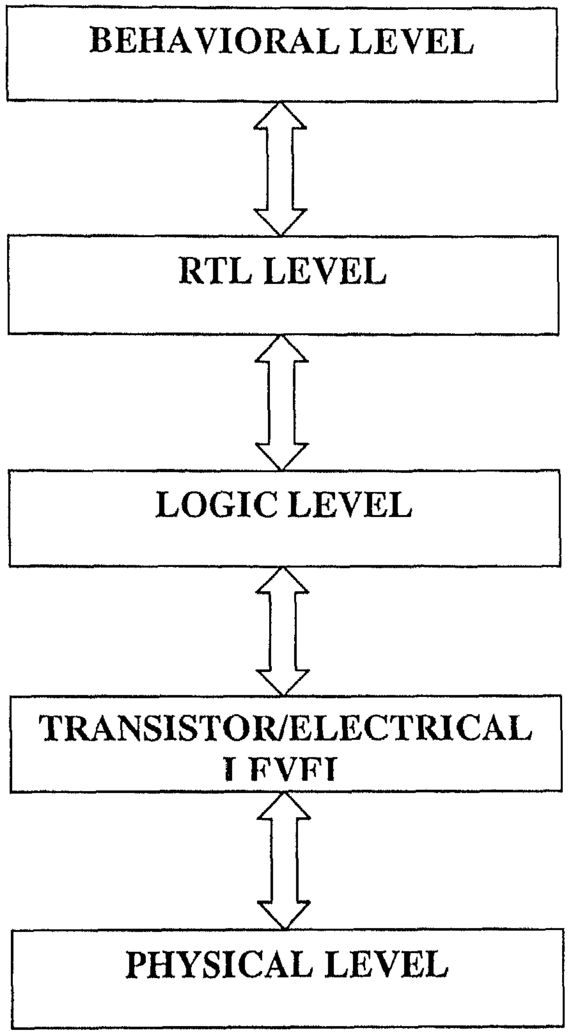


Figure 1 1 Design and Verification hierarchy

At the behavioral level the verification is carried out by just verifying the functional behavior At the RTL stage the verification is carried out by RTL simulators and these need to verify functional blocks like registers combinational and sequential blocks The RTL simulators provide more accurate information and may sometime also provide crude timing information as well These are helpful for data path design At the logic or gate level simulators check the circuit by evaluating the voltage or logic at each node by using the Boolean expressions of the gates These can provide first order timing details by inserting delays at the end of logic evaluation The actual rise and fall delays are calculated by using more accurate timing simulators that generally work at the transistor level and consider the layout and the technology dependent parasitics After the transistor level circuit is mapped to the physical level then a detailed extraction of the parasitics is done and the circuit specifications are again verified with these new values of parasitics

In each step, as the design is being mapped to the next level details are being added and hence the simulation at each level takes more and more time as we go down the design hierarchy but the accuracy increases

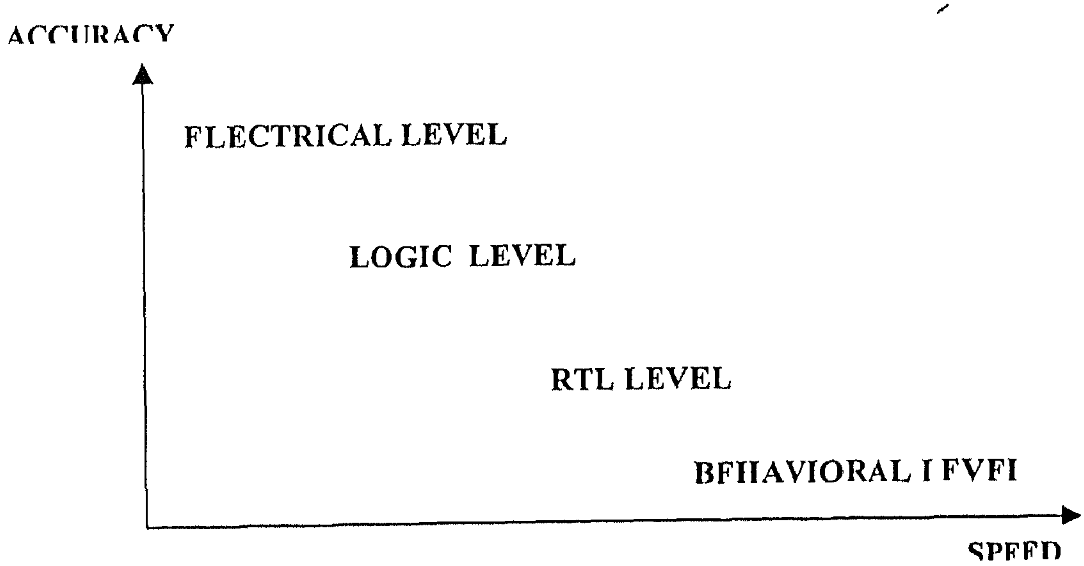


Figure 1 2 Levels of simulation and their respective speed of simulation

Electrical (transistor) level simulators like SPICE provide the most accurate information on the voltage waveform at the circuit nodes and the current through the circuit elements However these are computationally very intensive and take a lot of time and so their usage is limited upto a few thousand transistors

Inorder to bridge this gap between the slow but highly accurate electrical simulation and the fast but inadequate logic level simulation many intermediate level simulation levels have been incorporated like switch level logic simulation switch level timing simulation fast timing simulation and timing simulation All these have been explained in brief

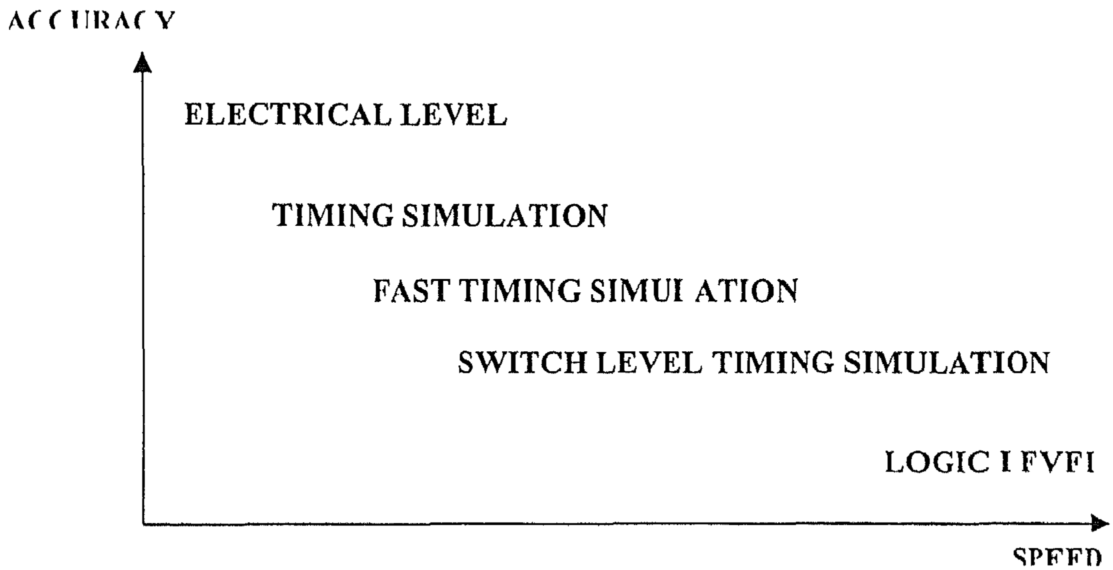


Figure 1 3 Intermediate levels of simulation

A switch level simulator is basically used to determine the steady state values of nodes and then to apply a delay operator if the steady state values change It considers the transistors to be switches, which are controlled by the voltage applied to the Gate terminal These are inaccurate The timing simulation is more accurate than a switch level simulation but they are still slow for very large digital circuits because they use the time point iteration techniques Fast timing simulations have been developed to account for

this gap between the switch level simulator and the timing simulator These have been made as accurate as the timing simulators but also fast enough for large circuits Several different approaches to fast timing simulation have been proposed but on a broad basis they have been made fast and accurate by the following features that they incorporate like

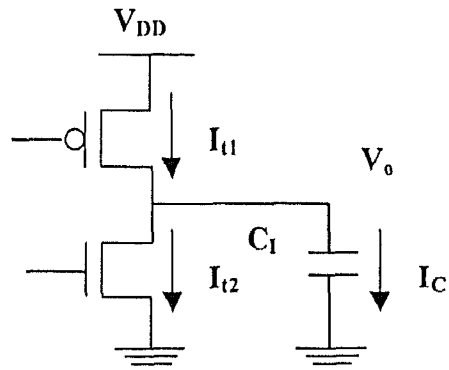
1 Event driven
2 Simplified Transistor models
3 Use of primitive or macro models to which sub circuits are mapped
4 Efficient use of analytical solution techniques for nodal differential equations
5 Waveform relaxation techniques for circuits with feedback

1 2 FAST TIMING SIMULATION

Since its inception, fast timing simulation techniques have been vastly improved, and the existing timing simulators are as accurate as conventional timing simulators Several different approaches have lead to different timing simulators They can however be broadly classified into two basic types The first type use integration formulae to convert the differential equations to difference equations and use a linear macro model to simplify and solve the differential equations The time steps in the simulation are usually small for obtaining accuracy and these are too inefficient to simulate large VLSI circuits Examples of this type of simulators include Elogic SPEC2 MOTIS3 MDCsim Event EMU and ADEPT The second type uses a nonlinear macro model or primitive and solves the differential equation governing node voltages analytically The non linear macro models provide accuracy and the analytical solutions provide the required efficiency These simulators have speed ups of the order of 3 magnitudes over SPICE2 and so from the point of view of efficiency are suitable for simulating large VLSI circuits Examples of this category are IDSIM2 and ILLIADS

ILLIADS incorporates all the above mentioned five concepts to achieve very good efficiency along with a considerable accuracy[2] In this the circuit is partitioned into blocks of MOS devices resistors and capacitors called as DCCBs (DC

connected blocks) and directed graphs are constructed The circuit graph is then condensed and the order in which the blocks need to be simulated is found and put in the correct temporal order for simulation and then as per the event driven methodology the simulation is done It uses primitives or macro models to which the circuit is mapped The circuit primitive used in ILLIADS is the generalization of the inverter macro model shown in Figure 1 4(a) The generic circuit primitive for MOS digital circuits is also shown in Figure 1 4(b) The primitive contains linear capacitances and resistances and parallel branches of NMOS and PMOS transistors Piecewise linear voltage sources are applied at the gate and drain terminals All the voltage dependent gate drain capacitances are lumped at the gate and drain/source nodes Also, the junction and overlap capacitances are lumped at the corresponding terminals of the MOS devices The resistive branches have been included in the circuit primitive for generality but do not occur in MOS digital circuits and so are excluded from simulation



(a) Inverter macro model (charging/discharging)

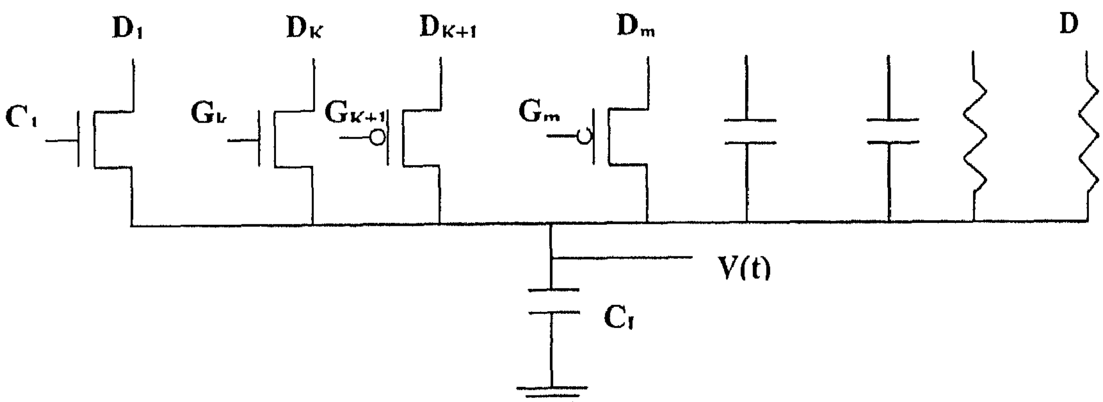


Figure 1 4 **(b)** Generic MOS circuit primitive in ILLIADS

1 3 NODE MERGING AND PRIMITIVE MAPPING

In a DCCB all the nodes can be categorized into four different types *resistive internal driven* and *pass* Resistive nodes are those which are connected to resistors capacitors and/or gate terminals of MOS transistors Internal nodes are the ones that connect the dc paths of only one type of transistor A driven node connects the dc paths of both NMOS and PMOS transistors and has a dc path to a voltage source that contains no other nodes apart from internal nodes All the other nodes are classified as pass nodes

In ILLIADS all internal nodes are eliminated by serial and parallel merging of transistors and finding an equivalent transistor and an equivalent gate signal For serial merging two transistors with transconductances β_1 and β the transconductance of the equivalent transistor is given by $\beta_1\beta_2/(\beta_1+\beta_2)$ and the equivalent gate signal is taken to be the weaker of the two gate signals Incase of parallel merging of two transistors the transconductance of the equivalent transistor is given by $\beta_1+\beta_2$ and the equivalent gate signal is given by the stronger of the two signals The internal node elimination can be done in two ways One way is to directly take the complete gate netlist and start eliminating the internal nodes by the serial and parallel merging technique The other is to first break the netlist into a net of NAND/NOR gates and then to replace each such gate by an equivalent inverter In ILLIADS the first technique is used Once the netlist has been reduced by eliminating internal nodes to the maximum extent it is mapped to the primitives available and the output computed

1 4 FOCUS OF THE WORK

In transistor merging the objective is to obtain the parameters of an equivalent transistor that reflects the I V characteristics of the serial or parallel combination In general this is a very difficult problem to solve analytically primarily owing to the complex nature of the MOS drain current equations and the complexity of the relationship between the drain current and the MOS model parameters As a result a number of assumptions are required to perform the merging A few of the most common

assumptions are to take the same model for all the transistors that need to be merged to neglect the channel length modulation and the parasitic capacitance effects and to take the same gate signal for all the transistors that need to be merged Though this procedure of finding the effective gate signal transconductance and channel length modulation works well for long geometry devices errors as large as 100% have been reported for sub micron devices [1] These errors have been found to arise in the serial merging of transistors with the errors being very low in parallel merging This is due to the effect of the internal nodes and the parasitic effects at these nodes in moderately to large number of serially connected transistors So it is important to take the effect of the internal nodes in the computation of the output waveforms

Lot of work has already been done in mapping the netlist to NAND/NOR gates and also an efficient and accurate enough technique of mapping serial transistors to an equivalent inverter has been reported in [1] In this the chain of serially connected transistors has been replaced by an equivalent transistor and only one parameter the width of the equivalent transistor has been computed to match it to the chain of transistors Also the model used for the transistor is the alpha power law model[3] which takes into account the velocity saturation effect which is one of the prominent short channel effects and thus results in more accurate results of the output Both the conducting as well as the parasitic behavior of parallel and serially connected transistors has been considered and an equivalent transistor extracted in each case taking into account the actual operation conditions of each device The modeling has been developed for non zero input transition times In order to map the input signals to an equivalent signal an input mapping algorithm has been proposed and also the weight of each transistor position in the gate structure has been extracted The algorithm of first collapsing a complex gate to an equivalent NAND/NOR gate and then mapping it to an equivalent inverter has been used The starting point of conduction of the transistor chain has been calculated to much accuracy and the equivalent transistor width has been calculated by fitting the actual output of the transistor chain to the output of the equivalent inverter Due to the analytical solution approach used in the paper the efficiency in calculating the equivalent inverter parameters is very high and the model

has been developed with the view to model the equivalent inverter using ILLIADS which is highly efficient

But in the calculation of the starting point of conductance the effect of substrate voltage (or the body effect) had been neglected which resulted in inaccurate values of the starting point of conduction Also the results for slow ramp inputs have shown more errors than for fast ramps In this approach the effective width has been calculated at a time that has been calculated from the starting point of conduction but then a different fitting parameters have been used for slow and fast ramps to get accuracy over a wide range of input transition times This has resulted in more errors for slow ramps than for the fast ramps

In this work the complete model for collapsing a series connected transistor chain to an equivalent transistor has been verified Also during the analysis for finding out the starting point of conduction the modulation of the threshold voltage due to the body effect has been taken into account and hence highly accurate results for the starting point of conduction have been obtained These have also resulted in very accurate results in the final output for slow ramps as well and the need for a different fitting parameter has been eliminated

Chapter 2
CMOS GATE MODELING

There are two techniques of modeling a gate The first method corresponds to the generalization of the inverter model and is based on a fully mathematical analysis of the gate structure This approach leads to a high mathematical complexity and hence less efficiency The second method utilizes the well established theory of inverters and research has been focused on the development of sophisticated methods for collapsing a CMOS gate into an effective equivalent inverter, whose output response will reflect accurately that of the gate The accuracy of this method is comparable to the former while the mathematical complexity is less resulting in better efficiency Several techniques have been developed for this second method of modeling the gate In order to map the gate to an equivalent inverter a delay degradation factor was introduced by Sakurai and Newton[5] while Nabavi Lishi and Rumin presented a semi emperical model[6] But all these have resulted in limited accuracy and finally for complex structures they have ended up in the conventional n times transconductance reduction for an n transistor chain

Recently the transistor chain characteristics has been studied from a macromodeling point of view In [1] a method for modeling CMOS gates by an equivalent inverter has been proposed In this approach the key points in the behavior of CMOS gates are modeled analytically in order to improve the accuracy of the final equivalent inverter, whose transistor's widths are calculated efficiently taking into account the mode of operation viz cutoff saturation and linear of the transistors in the gate Such key points are the starting point of gate conduction, which has a significant impact on the output waveform the form of the internal node voltages the parasitic behavior of the chain and the weight of each transistor position in the chain Also a very efficient algorithm for reducing each possible input pattern into an effective single equivalent input that can be applied to an inverter model has been proposed in this paper

In order to obtain the output voltage waveform at the output of a gate it needs to be mapped to an equivalent inverter Any complex gate is nothing but an interconnection of series and parallel combinations of transistors So for mapping any gate to an equivalent inverter serial and parallel transistors in the gate need to be collapsed into a single equivalent transistor As mentioned in section 1 4 the equivalent transistor for parallel transistors can be directly found out by adding up their transconductance and the errors introduced due to such a mapping are very low But for replacing a serially connected chain of transistors by an equivalent one the parasitic behavior and also the behavior at the internal nodes need to be considered to be able to get accurate results This technique as mentioned in [1] is described in the succeeding sections The input waveform for all the inputs of the chain has been considered to be the same and has been taken as a ramp input A mapping algorithm for mapping all the possible input patterns to an equivalent ramp input has been proposed for this in [1]

2 1 NMOS TRANSISTOR CHAIN MODEL

A gate can have a chain of PMOS or NMOS transistors So if the characteristics of one of the NMOS or PMOS chain are studied then the characteristics of the other will follow suit as they will be of the same nature So here a chain of NMOS transistors has been considered To replace a chain of transistors by an equivalent transistor the response of the chain was studied and the equivalent transistor chosen such that its response matches that of the chain To analyze the response of a chain of n NMOS transistors consider the circuit shown in Figure 2 1 (a), where the parasitic drain/source node capacitances are also shown An input ramp with transition time τ is assumed to be applied to the gates of all the transistors in the chain

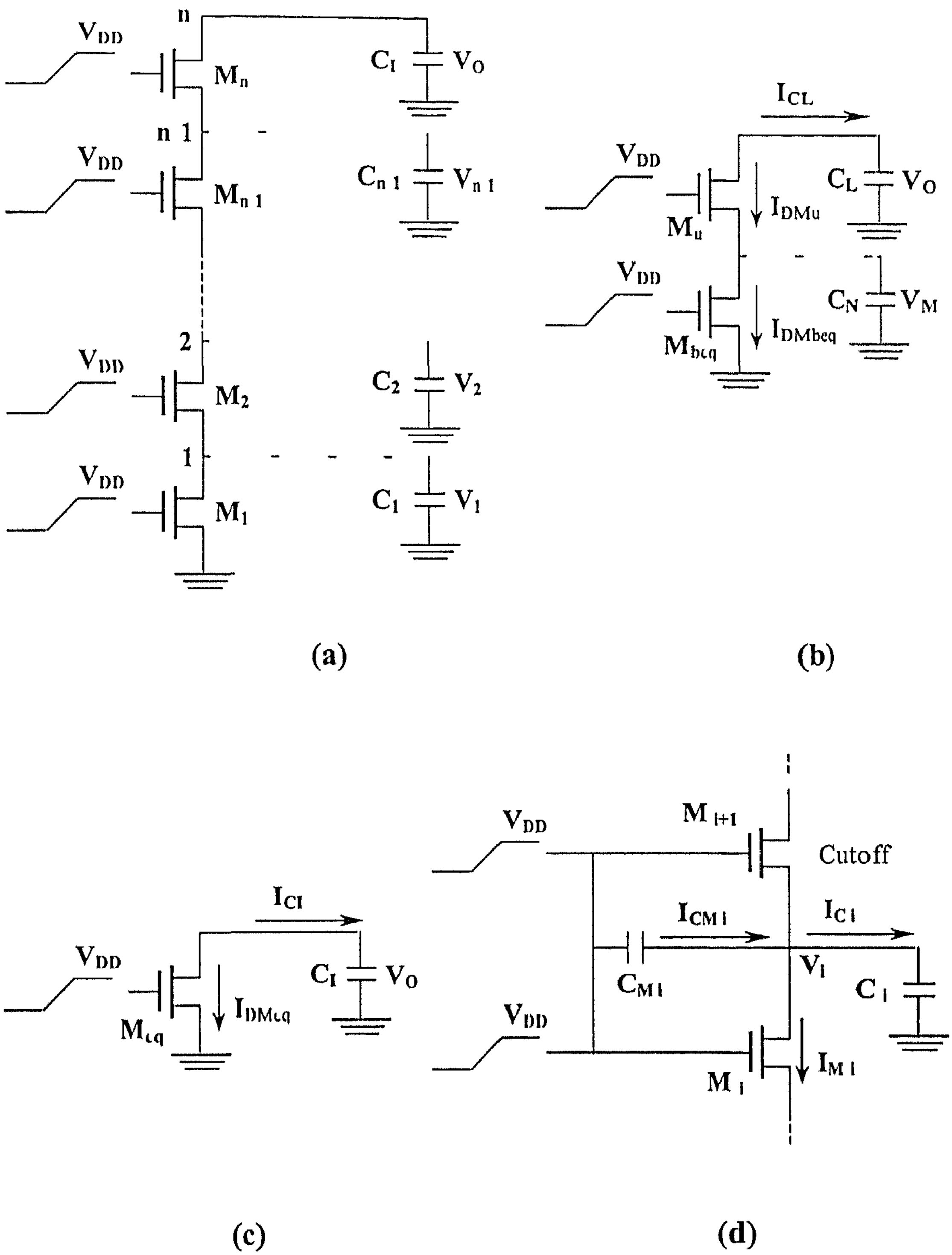


Figure 2 1 (a) Chain of n NMOS transistors **(b)** Two transistor equivalent model **(c)**Single equivalent transistor model **(d)** Currents at the ith node during $t_{s\,i}$ $t_{s\,i+1}$

The input ramp can be expressed as

$$V_{in} = \begin{cases} 0 & t \le 0 \\ \dfrac{V_{DD}}{\tau} t & 0 < t \le \tau \\ V_{DD} & t > \tau \end{cases} \qquad (2\ 1)$$

where τ is the time period of the ramp

In order to consider higher order effects the α power law model [3] which takes into account the carrier velocity saturation effect of short channel devices has been considered for the transistor currents The drain current according to this model is given by

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TN} \quad \text{cutoff region} \\ K_l (V_{GS} - V_{TN})^{\alpha/2} V_{DS} & V_{DS} < V_{D\,SAT} \quad \text{linear region} \\ Ks(V_{GS} - V_{TN})^{\alpha} & V_{DS} \ge V_{D\,SAT} \quad \text{saturation region} \end{cases} \qquad (2\ 2)$$

where $V_{D\,SAT}$ is the drain saturation voltage K_l K_S are the transconductance parameters which depend on the width to length ratio of the transistor α is the carrier velocity saturation index and V_{TN} is the threshold voltage expressed by its first order Taylor series approximation around $V_{SB} = 0\ 2V_{DD}$ as

$$\widetilde{V}_{TN} = V_{TN}|_{VSB=0\,2\,VDD} + (V_{TN})\,|_{VSB=0\,2\,VDD} \;(V_{SB} - 0\ 2\ V_{DD}) = \theta + \delta\, V_{SB} \qquad (2\ 3)$$

where V_{SB} is the source to substrate voltage i e the body voltage

The Taylor series has been calculated around $V_{SB} = 0\ 2\ V_{DD}$ since the voltage was found to lie close to the midpoint of the voltage swing of the source node of the top most transistor which is of primary importance to the proposed analysis A detailed derivation is given in the Appendix The whole transistor chain of Figure 2 1 (a) can be reduced to two transistors based on their behavior where in the top most transistor M_n is been left untouched and the remaining transistors mapped to an equivalent transistor as shown in

Figure 2 1 (b) The single transistor equivalent will be as shown in Figure 2 1 (c) The reason is as follows

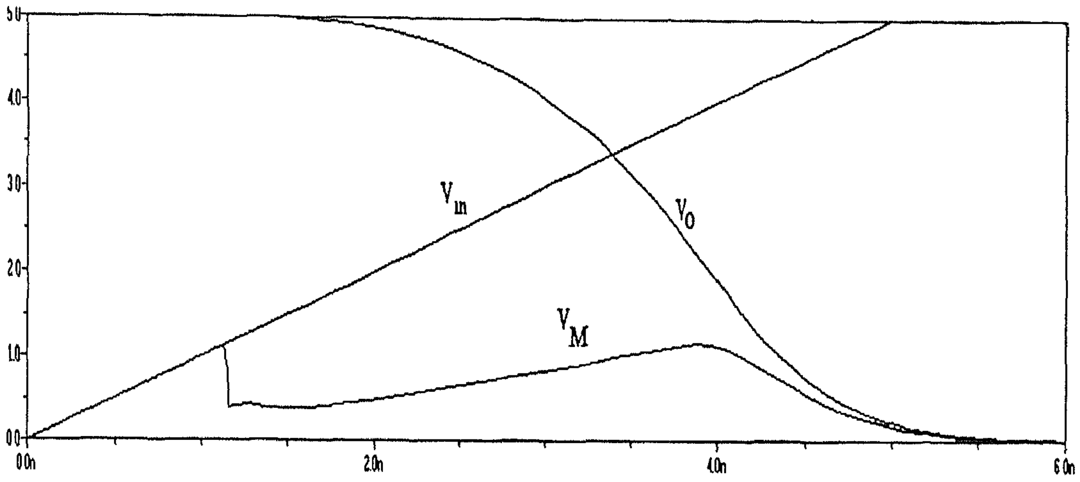
Let the voltage at the source of the top most transistor i e at the node n 1 be V_M which is a function of time While the input is applied and considering all the internal nodes to be initially discharged all the transistors will be cut off at the beginning as the gate voltage of all the transistors will be less than the zero body bias threshold voltage, V_{TO} But owing to parasitic capacitances (as shown in Figure 2 1 (d)) the voltages at the intermediate nodes (0 to n 1) begin to rise due to the current I_{CMi} At some time when the input voltage reaches V_{TO} the bottom most transistor M_1 goes into conduction by entering into the saturation region All the other transistors will be cut off as their source voltages are greater than zero (and hence less V_{GS}) due to the charging of the parasitic capacitances C_i Now as the transistor M_1 provides a discharge path for C_i the voltage at node 1 begins to fall and also as the gate voltage is increasing a point will come when its drain source voltage will become equal to the gate source voltage and so it will enter the linear region At this very instant the gate to source voltage of the transistor above it will be V_{TO} If we neglect the body effect then the transistor will enter into conduction by going into saturation at this instant Even with the body effect considered which will modulate the threshold voltage the upper transistor will enter into conduction somewhere near this point as the modulation of the threshold voltage will be very less

This process will continue and when the top most transistor (and hence the whole chain) enters into conduction with the top transistor going into saturation all the bottom transistors will be in the linear region The top most transistor operates in the saturation region for some time and when its drain source voltage becomes equal to the $V_{D\,SAT}$ it enters linear region while the transistors below it always remain in the linear region throughout this period So from the time at which the whole chain starts conduction the top most transistor experiences two regions of operation i e the saturation as well as the linear region while the transistors below it will always operate in the linear region All the bottom transistors as they behave identically can be replaced by an equivalent transistor and the top transistor which operates in two regions need to be handled

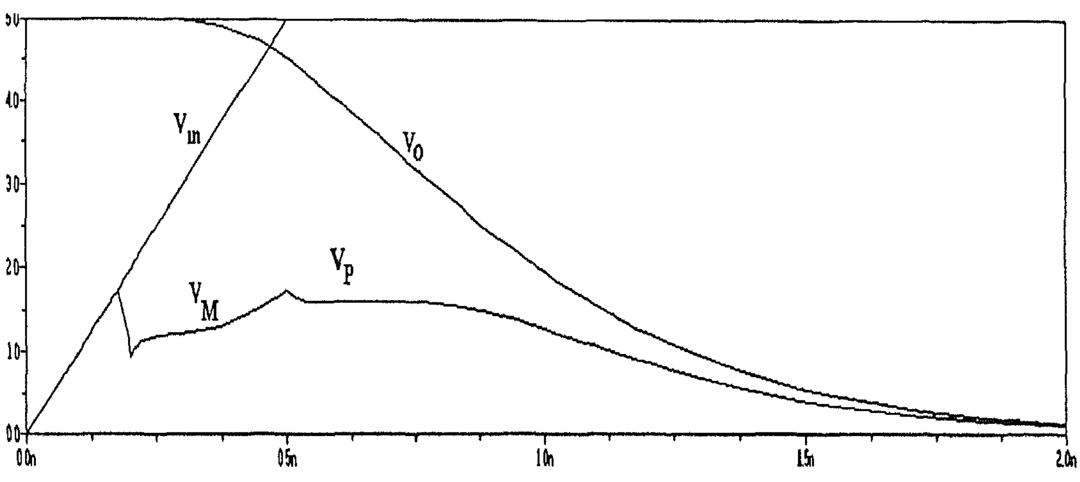
differently So the whole chain is first collapsed to a two transistor equivalent with the top transistor left untouched and all the bottom transistors replaced by a single equivalent transistor and then they are collapsed to an equivalent transistor Since the idea is to find out the equivalent transistor by analytical method the equivalent transistor has been found out by observing the output waveform at the node n 1 which corresponds to the output of the lower n 1 transistors The effective width of the transistor is computed to get the same response The voltage of the output waveform from the time the whole chain starts conducting say t_1 to the time at which the upper transistor enters linear region say t_2 has been found to be linear and rising to a voltage called as the plateau voltage

2 2 PLATEAU VOLTAGE

From the time interval during which the top most transistor (M_n) enters the saturation region and the input is rising its current and consequently the voltages at the internal nodes are increasing When the input reaches V_{DD} and till the time the top most transistor exits saturation (if it has not already done so) its current and hence the internal node voltages remain constant This is because the gate voltage is constant (V_{DD}) and so the drain current of the top most transistor which is in saturation will be constant Suppose the internal node voltages rise owing to a difference in the charging and the discharging currents of the parasitic capacitances then the voltage at the source of the top most transistor will also rise which will cause a reduction of its gate source voltage This will decrease its drain current and hence the charging current for the internal nodes So the voltage will drop again Now, suppose the voltage at the internal nodes try to decrease then due to the increase in the gate source voltage of the top most transistor, the drain current will increase charging up the nodes and thereby increasing their voltages So the voltages at the internal nodes will remain the same as long as the top most transistor remains in saturation after the input has reached the maximum value of V_{DD} This state is known as the *plateau* state and during this time the same current flows through all the transistors in the chain Figure 2 2 (b) shows the occurrence of plateau voltage (V_P) and is the output obtained by SPICE



(a)



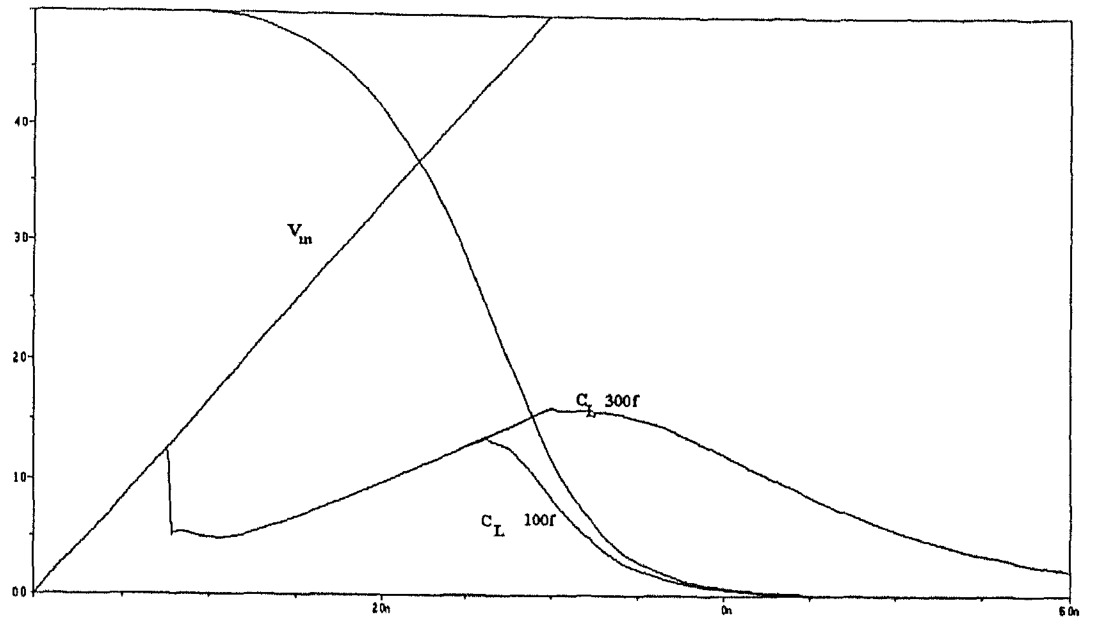
(b)

Figure 2 2 (a) Waveform at the node n 1 for a slow ramp

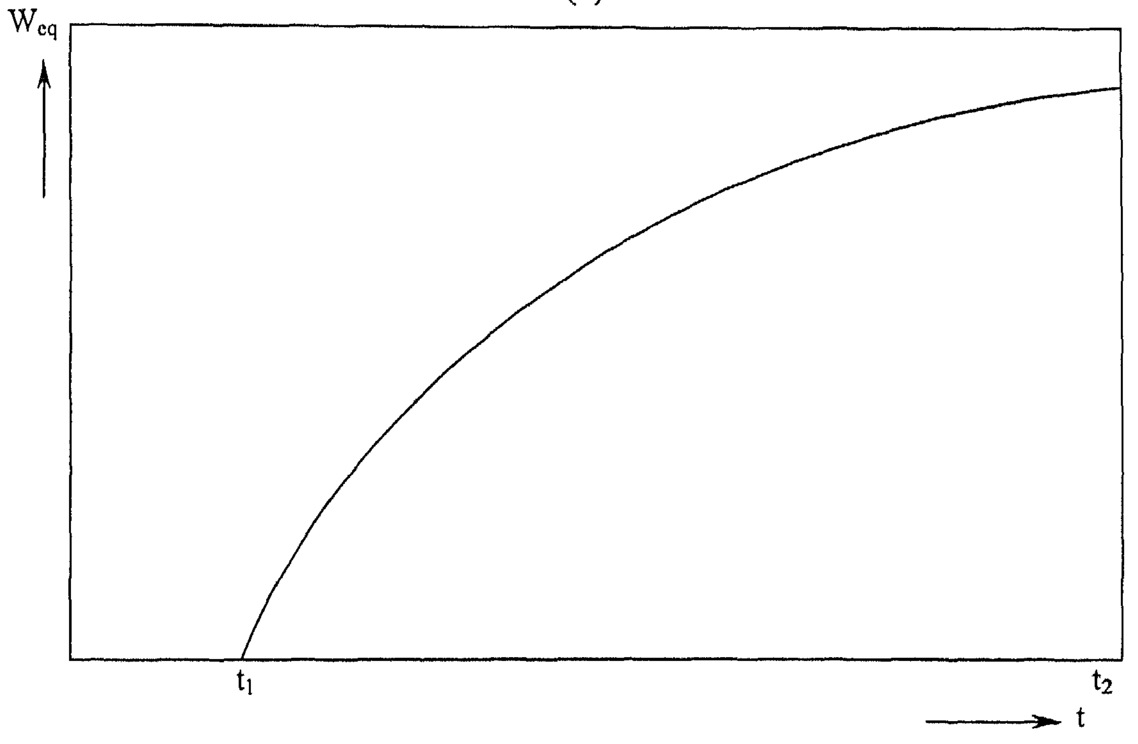
(b) Occurrence of Plateau voltage at the node n 1 for a fast ramp

Now we have seen that for the plateau state to appear the top most transistor must still remain in saturation region even after the input has reached the maximum of V_{DD} This can obviously happen when the input ramp is fast enough that it can reach V_{DD} before the top most transistor exits saturation So the plateau voltage appears only for fast inputs Fast and slow inputs are classified according to when the time at which the top most transistor exits saturation (t_2) occurs If $t_2 > \tau$ then it is a fast ramp (shown in figure 2 2 (a)) and if $t_2 < \tau$ then it is a slow ramp (shown in figure 2 2 (b)) For slow ramps the top most transistor enters linear region before the end of the ramp and the voltage at its source starts to fall before the plateau voltage can be reached Now the time at which the top most transistor enters linear region from the saturation region depends on when its drain source voltage drops below the $V_{D\ SAT}$ This depends on how fast the load capacitance C_L is discharging Suppose if the load capacitance were large enough that $V_{D\ SAT}$ is reached after the end of the ramp then the plateau voltage can be reached One observation that has been made by looking at the output of SPICE waveforms is that the slope of the voltage at the source of the top most transistor i e node n 1 remains constant between time t_1 and t_2 whatever be the load capacitance This is because we are considering the slope at a time when the top transistor is in saturation and in saturation the current depends only on the gate source voltage and not on the drain source voltage So the current will be the same in saturation for any load capacitance and so, the voltage at all the nodes below this transistor will follow the same characteristics for any load capacitance This has been shown in figure 2 3 (a) So whether the ramp is a slow one or a fast one we can always assume the load capacitance to be large enough and hence that the voltage at node n 1 reaches the plateau voltage

It should be noted that the effect of the channel length modulation has been neglected in the calculation of this plateau voltage Since channel length modulation specifies that even in saturation the drain current is dependent on the drain source voltage considering it will cause increase the complexity and will result in iterative equations So, it has been neglected and the errors have been found to be insignificant when compared to the results of SPICE



(a)



(b)

Figure 2 3 (a) Waveform at the node n 1 for different load capacitances

(b) Variation of the single transistor equivalent width with time during the saturation period of the top most transistor

In order to calculate the plateau voltage V_P at the source of the top most transistor of the chain consider the circuit shown in Figure 2 1 (a) The plateau voltage occurs at the end of the input ramp when $V_{in} = V_{DD}$ and the current ceases to increase Thus V_P can be calculated by setting the saturation current of the top most transistor (M_u) equal to the current of the bottom transistor (M_{beq}) shown in Figure 2 1 (b) which operates in the linear mode

$$K_{su}\,(V_{DD} \quad \theta \quad (1+\delta)V_p\,)^{\alpha} = K_{lbeq}\,(V_{DD} - V_{TO}\,)^{\alpha/2}\,V_P \tag{2 4}$$

The equation can be solved with very good accuracy using second order Taylor series approximation The solution has been explained in detail in Appendix

2 3 EQUIVALENT WIDTH

A single equivalent transistor will be able to replace a transistor chain if it manages to have the same output response as that of the combined behavior of the chain with the dual operation of the top transistor in saturation as well as linear region For the time interval that the top transistor is in saturation the current through the top transistor is the bottleneck for the current that is flowing through the complete chain So the equivalent width (W_{eq}) of the single equivalent transistor M_{eq} as shown in Figure 2 1 (c) during this time can be obtained by equating the current through the top most transistor to the current through the equivalent transistor

$$I_{Mn} = I_{Meq}$$

$$\Rightarrow P_s \frac{W_n}{L}(V_{in} - \theta - (1+\delta)\,V_M)^{\alpha} = P_s \frac{W_{eq}}{L}(V_{in} - V_{TO}) \tag{2 5}$$

The above equation can be solved for different values of t yielding corresponding values of W_{eq} values For the time interval $[t_1, t_2]$ for which the top transistor operates in saturation W_{eq} plotted against time has the form as shown if Figure 2 3(b) In order to find the average effective value of W_{eq}, the time point t_2 needs to be calculated This can be done by solving the following equation at the output node *n* (detailed solution is given in Appendix II)

$$V_{D\,SATn}[t_2] = V_{out}[t_2] - V_M[t_2] \tag{2 6}$$

It must be noted that in the calculation of t the effect of the parasitic short circuit current of the PMOS transistor structure during the switching action has been neglected This has been done purposefully to keep the mathematical complexity low The effect of this parasitic current is to add some more charge to the load capacitance and thus extend the saturation region This will affect the W_{eq} calculated and so to keep the complexity low instead of adding the expression of the current of the PMOS transistor structure the effective W_{eq} has been chosen so as to compensate for these parasitics SPICE results have shown that the bound on the saturation region due to these parasitic currents depends on the input slope and the load capacitance This can be the result of the increase in short circuit current as the input transition time increases and as the output load capacitance decreases A very good approximation found valid for a wide range of input slopes and capacitances is to calculate the W_{eq} at time $t = t_2$ for fast inputs and at $t = (t_1+3\ 3t_2)/4$ for slow inputs where t_1 is the time at which the complete chain starts to conduct This W_{eq} corresponds only to the region where the top most transistor is in saturation and so will be referred to as W_{sat} If there is no parasitic action of the PMOS chain then W_{eq} is calculated at $t = (t_1+t_2)/2$ As this equivalent width has been calculated for the time when the top most transistor operates in the saturation region from now on it is referred as W_{sat}

$$W_{sat} = W_{eq}[t]$$

Where $t = (t_1+3\ 3t_2)/4$ Slow ramps

$t = t_2$ Fast ramps **(2 7)**

When all the transistors operate in the linear region, the transistor chain acts as voltage divider with a uniform distribution of the output voltage among all the drain/source nodes So the W_{eq} for the time for which the top most transistor is in the linear region can be just calculated as the average of the widths

As the effective width of the equivalent transistor for each region is now known the chain can be modeled by a single transistor whose effective width is W_{sat} from time t_1 to t_2 and for the rest of the time is W_{lin} But as the aim is to provide an equivalent width that would match the existing inverter models the above two widths need to be merged

into one This can be done by calculating the effective charge that is discharged to the ground in each case Then weights can be attached to each of the effective widths to calculate the overall equivalent width as

$$W_{eq} = C_{sat} \; W_{sat} + C_{lin} \; W_{lin} \tag{2 8}$$

Where

$$C_{sat} = Q_{sat} / Q_{total}$$
$$C_{lin} = 1 \quad C_{sat} \tag{2 9}$$

Where Q_{total} is the total charge that is stored initially in the output load and is given by

$$Q_{total} = C_L \; V_{DD} \tag{2 10}$$

Q_{sat} is the fraction of charge that is discharged to ground during the time in which the top transistor in the chain operates in saturation and is given by

$$Q_{sat} = Q_{total} - Q[t_2] \; = \; C_L \; V_{DD} - C_L \; V_o[t_2] \tag{2 11}$$

Note that in the above equations (2 5) and (2 6) V_M is a function of time In order to know the function V_M we need to know the points (V_1 t_1) and (V_2 t_2) or (V_P τ) since V_M is a linear function of time passing through these points as shown in Figure 2 2(a) and Figure 2 2(b) Of these V_P has already been calculated and τ is nothing but the time period of the input ramp So V_1 and t_1 remain to be calculated and then V_M can be formulated as

$$V_M(t) = V_1 + m \; (t - t_1) \tag{2 12}$$

Where m the slope of V_M is given by

$$m = (V_P \; V_1) / (\tau \; t_1) \tag{2 13}$$

2 4 STARTING POINT OF CONDUCTION

In a transistor chain with initially discharged internal nodes and the same input applied to the gates of all transistors the closer to the ground transistors start conducting first and then the top transistors follow So in order to be able to model efficiently the

chain by an equivalent transistor the starting point of conduction of the chain which is actually the starting point of conduction of the top most transistor needs to be calculated

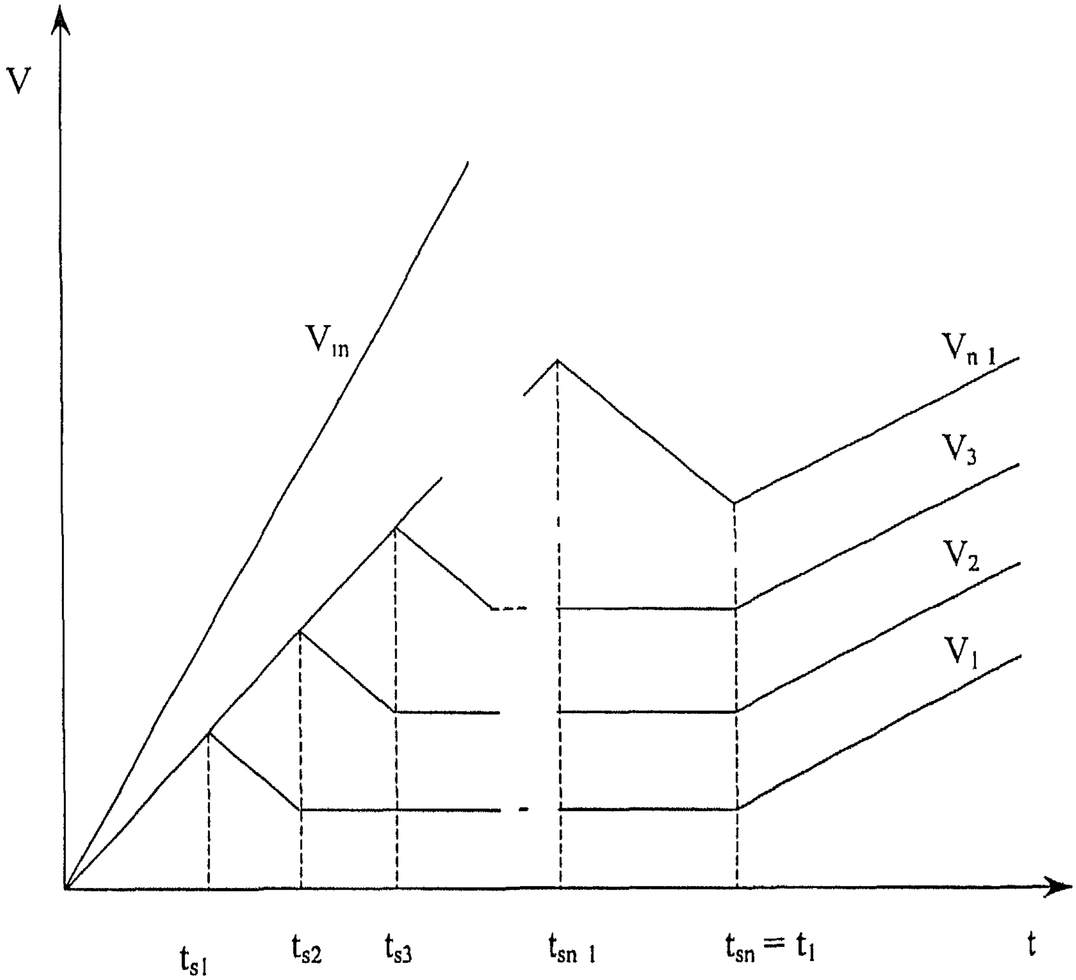


Figure 2 4 Internal node voltage waveforms till the complete chain starts conduction

The voltage waveforms at the internal n 1 nodes of an n transistor chain when the same input is applied to all the inputs are shown in Figure 2 4 When the input is applied initially all the transistors remain cut off as the gate voltage of all the transistors will be less than V_{T0} But owing to parasitic coupling capacitances (as shown in Figure 2 1 (d)) the drain voltages tend to follow the input ramp due to the current I_{CMi} The coupling

capacitances arise due to the gate source and the gate drain overlap capacitances of the upper and lower transistors respectively and are given by

$$C_{overlap} = W[C_{gdo} + C_{gso}] \tag{2 14}$$

where W is the transistor width and C_{gdo} and C_{gso} are the gate drain and the gate source overlap capacitances per micron which are determined by the process technology

Until the time when the input voltage reaches V_{TO} and when the bottom most transistor M_1 goes into conduction by entering the saturation region the nodes are isolated between the two cutoff transistors So the voltages at all the nodes can be obtained by equating the current due to the coupling capacitance I_{CM_1} at the node 1 with the charging current of the parasitic node capacitance I_{C_1} (Figure 2 1 (d))

$$I_{CM_1} = I_{C_1}$$

$$\Rightarrow C_M \frac{dV \;\; - dV}{dt} = C_I \frac{dV}{dt}$$

$$\Rightarrow V\,[t] = \frac{C_{M_1}}{C_M + C_I} V\;\;[t] \tag{2 15}$$

Since the input ramp has been considered to have a time period τ at the time t_{s1} when M_1 goes into conduction the input will reach V_{TO} So, t_{s1} can be calculated as

$$t_{\,1} = V_{TO} \frac{\tau}{V_{DD}} \tag{2 16}$$

All the other transistors will be in cutoff as their source voltages are greater than zero due to these node voltages Now as M_1 transistor provides a discharge path the voltage at node 1 begins to fall and also as the gate voltage is increasing a point will come when its drain to source voltage will become equal to the gate source voltage and so it will enter the linear region At this very instant the gate to source voltage of the transistor above it will be V_{TO} So if we neglect the body effect then it will enter into conduction by going into saturation at this instant Even with the body effect considered, which will modulate the threshold voltage the upper transistor will enter into conduction

somewhere nearer to this point as the modulation of the threshold voltage will be very less

After the time the bottom transistor M_1 starts to conduct (t_{s1}) and the time the complete chain starts to conduct (t_l) the node 1 will be subject to two opposite trends One tends to pull the voltage at the node up due to the charging through the coupling capacitance which is intense for fast inputs while the other is to pull it down to zero by the discharging current through the transistor (i e its drain current) Initially M_1 enters the conduction region by operating in the saturation region (since its V_{DS} is greater than its V_{GS} which is near zero) Since the gate drain coupling capacitance in will be small the charging rate will be less Due to the high rate of discharging the second of the trends dominates and the voltage at the node 1 will begin to fall This will continue till the time when the transistor M_1 will enter the linear region (at t_{s2}) At this very instant the second transistor will enter into conduction as its gate source voltage approaches V_{TO} From this time onwards the gate source capacitance of the second transistor and the gate drain capacitance of the bottom transistor will increase (This happens because the overlap capacitances depend on the region of operation The actual relation is given in Appendix), and so the rate of charging will also increase It has been observed by SPICE simulations that during the time at which the second transistor enters into conduction (saturation) and the whole chain starts to conduct, these two opposite trends seem to balance each other and the node voltage almost remains constant At the time when the third transistor enters into conduction the same process happens at the node 2 and in general at all the internal nodes the same process happens and the output waveforms will be as shown in Figure 2 4

This process will continue and when the top most transistor (and hence the whole chain) enters conduction by going into saturation at time ($t_{sn} = t_l$) the node voltages begin to rise Another observation which has helped in getting at the value of t_l is the slopes of these internal node voltages As can be seen from the graph which has been verified by SPICE the slopes of the node voltages during the time [t_{si} t_{si+1}] are almost same for all the transistors and so this assumption has been considered which is a safe

one without ending up in significant errors This slope say m can be derived by solving the differential equation which results from the Kirchhoff's current law at node 1 (Figure 2 1 (d))

$$i_{M1} = i_{CM1} \quad i_{C1}$$

$$\Rightarrow K_S \, (V \quad -V_{TO}) = C_{M1}\left(\frac{dV}{dt} - \frac{dV_1}{dt}\right) - C_1\left(\frac{dV_1}{dt}\right) \qquad (2\,17)$$

Here for simplicity, the velocity saturation index α has been considered to be one

To get the average slope say r of the node voltages during the time [t_{si} t_{si+1}] the time points t_{s1} t_{s2} and the corresponding drain voltage (node voltages at the node 1 for these two time points) need to be calculated We already have t_{s1} from equation (2 16) and the corresponding node voltage from equation (2 15) Since at time t_{s2} the second from bottom transistor M_2 starts conducting the time t_{s2} can be calculated by solving the equation

$$V_{GS}[t_{s2}] = V_{TN2}[t_{s2}] \qquad (2\,18)$$

So from these values r can be calculated Similarly by using the equation (2 18) the time points at which the other transistors enter into conduction can be calculated The starting point of conduction of the whole chain i e t_i can be calculated by solving the following equation

$$V_{GS}[t_{si}] \quad V_{TNi}[t_{si}] = 0$$

$$\Rightarrow (V_{in}[t_{si}] \quad V_S[t_{si}]) - (\theta_0 + \delta_0 V_S[t_{si}]) = 0 \qquad (2\,19)$$

Where $V_S[t_{si}]$ is the voltage (with respect to ground) at the source of transistor i at time t_{si} and can be calculated as

$$V_S[t_{si}] = \frac{C_{Mi\ 1}}{C_{Mi\ 1} - C_{i-1}} V_i\ [t_{si\ 1}] - r(t_{si} - t_{si\ 1}) \qquad (2\,20)$$

The constants θ_0 and δ_0 are the ones obtained from the equation (2 3) for V_{SB} = V_{TO} for higher accuracy because the node voltages lie close to V_{TO} and not around 0 $2V_{DD}$ as in equation (2 3)

Equation (2 19) results in a recursive expression for t_{si} and is given as

$$t_i = \tau \frac{\theta_0 + (1+\delta_0)\left(\frac{C_{M\ 1}}{C_{Mi\ 1}+C_{\ 1}}\,\frac{V_{DD}}{\tau} + r\right) t_{\ 1}}{V_{DD} + (1+\delta_0)\, r\, \tau} \qquad i \geq 2 \qquad \textbf{(2 21)}$$

And t_l will be equal to t_{sn} Thus having obtained t_l all the above equations can be solved and thus the effective width W_{eq} of the equivalent single transistor that can replace the complete chain can be obtained

2 5 DISCUSSION

It should be noted that in the calculation of t_l while calculating the value of t_{si} and thus t_l the effect of body voltage has not been considered Due to this some error in the calculation of t_l arises and as the number of transistors in the chain increases this error increases because the body effect affects the values of all t_{si} values and hence as n increases the error introduced also increases So though the method of finding the value of t_l as discussed above is a simplified approach and finds the value analytically it has resulted in errors which could have been avoided had the body effect been considered In the next chapter analysis has been done to find out the value of t_l more accurately by considering this body effect Also while doing this computation care has been taken to see that the extra calculations involved do not reduce the efficiency of the overall computation, since the idea is to implement it into a fast timing simulator

Chapter 3

IMPROVED CMOS GATE MODELING CONSIDERING THE BODY EFFECT

3 1 BODY EFFECT

During fabrication all the MOS devices are fabricated on a single substrate As a result, the substrate voltage of all the devices will be the same So when a number of transistors are connected in series, the source substrate voltage of all the transistors will not be equal and it will increase as we proceed vertically in the chain During the operation of a MOS transistor when V_{GS} is greater than its threshold voltage the depletion width remains constant and charge carriers are pulled into the channel from the source But as the substrate bias is increased the width of the channel substrate depletion layer also increases resulting in an increase in the density of the trapped carriers in the depletion layer to maintain the charge neutrality the channel charge must decrease The result is that the body voltage adds to the channel substrate junction potential This increases the gate channel voltage drop The overall effect is an increase in the threshold voltage Therefore the threshold voltage is no more constant with respect to the source substrate voltage This effect of modulation of the threshold voltage by the substrate bias is called as the *substrate bias effect* or the *body effect* The relation between the threshold voltage to the substrate voltage is given in Appendix I and has been used in equation (2 3)

3 2 EFFECT ON THE STARTING POINT OF CONDUCTION

In the analysis carried out in the previous chapter, the body effect had been considered for calculating the V_{TN} for all the transistors in the transistor chain But in the modeling done for finding out the starting point of conduction the idealization of the output that has been done as in Figure 2 4 is valid only if the body effect is not taken into consideration In the Figure 2 4 the transistor M_2 has been said to go into conduction exactly at the time the bottom transistor enters linear region from the saturation region This means that the threshold voltage of this transistor is equal to V_{TO} i e the body effect

has not been considered or that its body substrate voltage is zero This should mean that the substrates of all the transistors are tied to their respective source terminals and this will result in a circuit as shown in the Figure 3 1 (a) The waveforms at the internal nodes of such a chain obtained by SPICE level 3 simulations are shown in Figure 3 2 (a) From this graph it is clear that the waveforms are falling linearly during the time [t_{si} t_{si+1}] and exactly at the time the node voltage becomes constant the transistor above it is entering into conduction This validates the idealization done in Figure 2 4

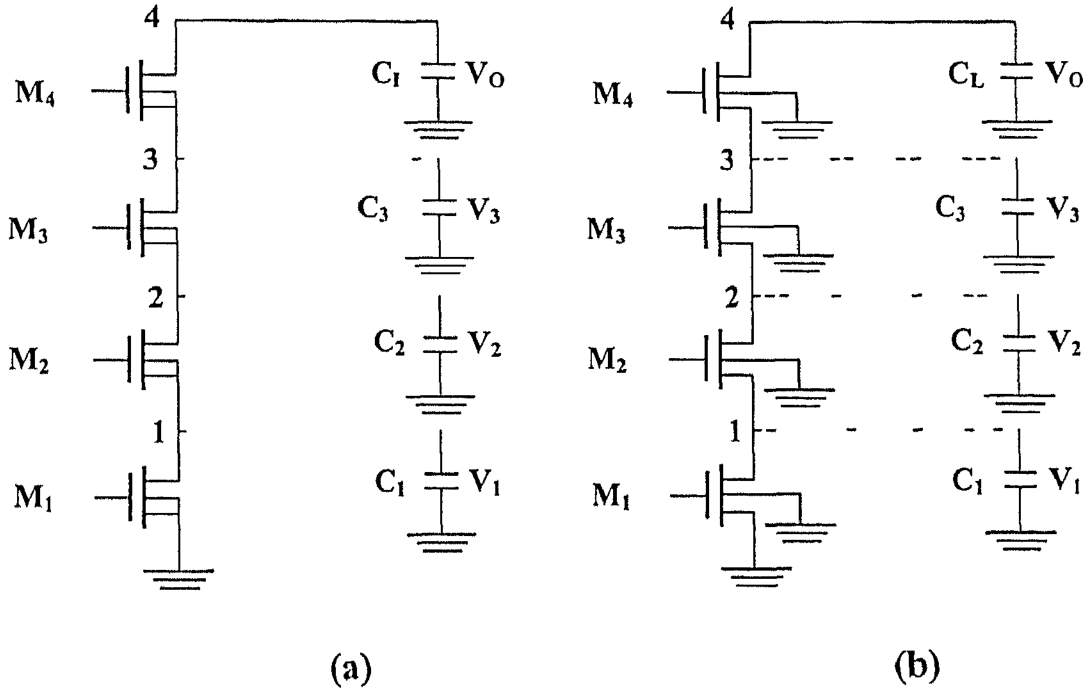
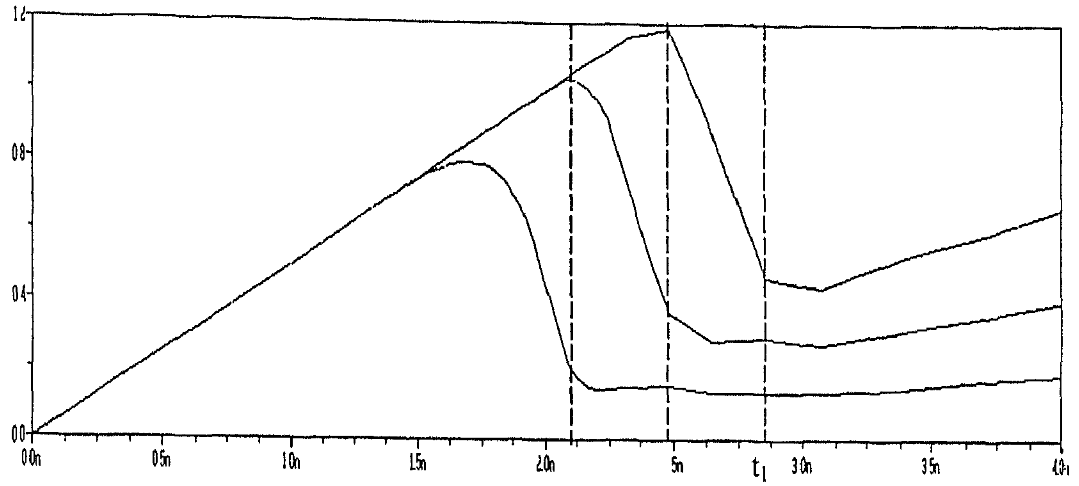
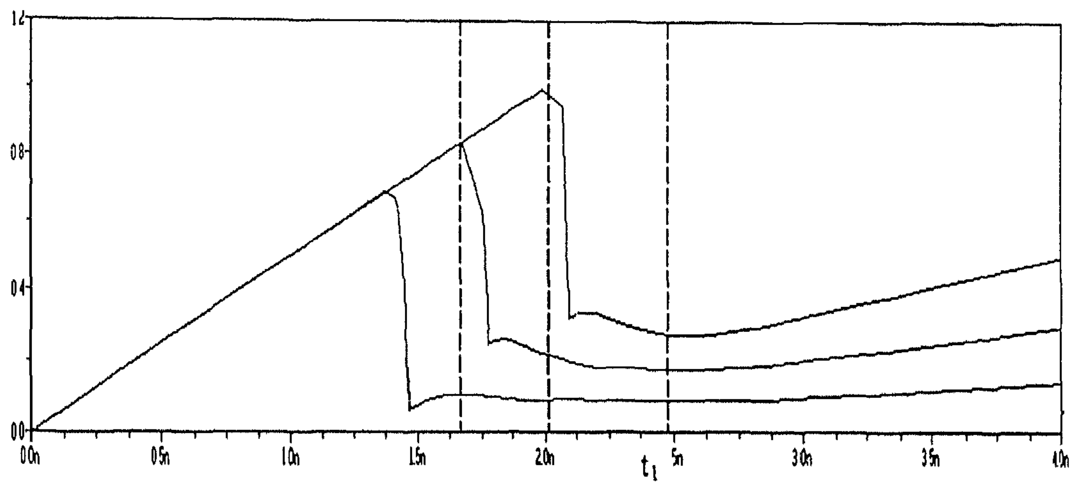


Figure 3 1 (a) Chain of 4 transistors with substrate of each transistor connected to its source terminal **(b)** Chain of 4 transistors with a common substrate which is grounded



(a)



(b)

Figure 3 2 (a) Output of a chain of 4 transistors without considering the body effect
(b) Output of a chain of 4 transistors considering the body effect

But in practice the type of chains that are encountered are of the form shown in Figure 3 1 (b) wherein the substrate for all the transistors is common and so is at the same potential This causes the threshold voltage of all the transistors to be different and it increases as we move up the chain due to the increasing source body voltage When the bottom transistor enters the linear region the V_{GS} of the transistor above it will be equal to V_{TO}, but still as its V_{TN} will be greater than V_{TO} it will not enter into conduction The result is that the bottom transistor will operate in the linear region for sometime during which its drain voltage will be still falling but at a different rate before the transistor above it enters into conduction Once the upper transistor starts conducting then the analysis mentioned in the previous chapter holds good and the drain voltage of the bottom transistor will almost become constant During the time that the bottom transistor is in linear region and the transistor above it is not conducting the rate of fall of the drain voltage of the bottom transistor will be different from the rate at which it was falling when the transistor operated in the saturation region The result is that the linear approximation taken in the previous chapter for this region is no longer valid To get accurate results the region will have to be broken up into two different parts and modeled separately with the first region modeled as before with the bottom transistor in saturation and the second region modeled with the bottom transistor in linear region The output of the internal nodes of a 4 transistor chain with a common substrate, as shown in Figure 3 1 (b), obtained by SPICE level 3 modeling is shown in the Figure 3 2 (b) The late occurrence of the starting point of conduction of the transistors in the chain from the time the bottom transistor exits the saturation region is pretty clear from the graphs

3 3 PWL MODELING FOR STARTING POINT OF CONDUCTION

In the previous analysis we had assumed that the transistors operate only in the saturation region from the time they start conduction to the time the transistor above it starts conduction This helped in increasing the efficiency of the computation because in saturation the current as well as the parasitic capacitances is independent of the drain source voltage and what we are trying to find out is the drain source voltage itself (node

voltages) Once we divide the region into two regions we can again easily calculate the values related to the saturation region But in the calculation of the values related to the linear region the computations become iterative because the drain current and the parasitic capacitances (Refer Appendix I) are now dependent on the drain source voltage which is exactly what we want to compute In doing so though the accuracy is increased we have to sacrifice lot of computational efficiency Instead of going for iterative expressions we can make some assumptions which can reduce the equations to ordinary quadratic expressions without sacrificing much of the efficiency The assumptions that have been taken are not just taken to fit to the data but have been done by studying the output response of the waveforms obtained by SPICE 3 simulations By looking at the waveforms of Figure 3 2 (b) it can be seen that the slope of the waveform from the time a transistor goes into conduction by entering into saturation to the time it goes into the linear region is same for all the transistors (same as the assumption taken in the previous chapter) Similarly the waveform from the time the transistor enters the linear region to the time the transistor above it starts conduction can be approximated by a straight line and also the slope for all the transistors is nearly the same This simplification will lead to the reduction of the Figure 3 2 (b) to that shown in the Figure 3 3 for a general n transistor chain

So if say that the average slope of the waveform for the time $[t_{si}\ t_{li}]$ is r and that for the time $[t_{li}\ t_{si+1}]$ is s, then we need to calculate the voltage at the drain of the bottom transistor for the time points t_{s1} t_{l1} and t_{s2} and from these r and s can be obtained Once we have these values then using them, we can easily find out the time point t_i So the PWL approximation of the output waveform at the nodes of the transistor chain and the assumption that the average slopes for the time $[t_{si}\ t_{li}]$ and $[t_{li}\ t_{si+1}]$ are same for each node, helps a lot in simplifying the complexity involved in the calculation of the starting point of conduction

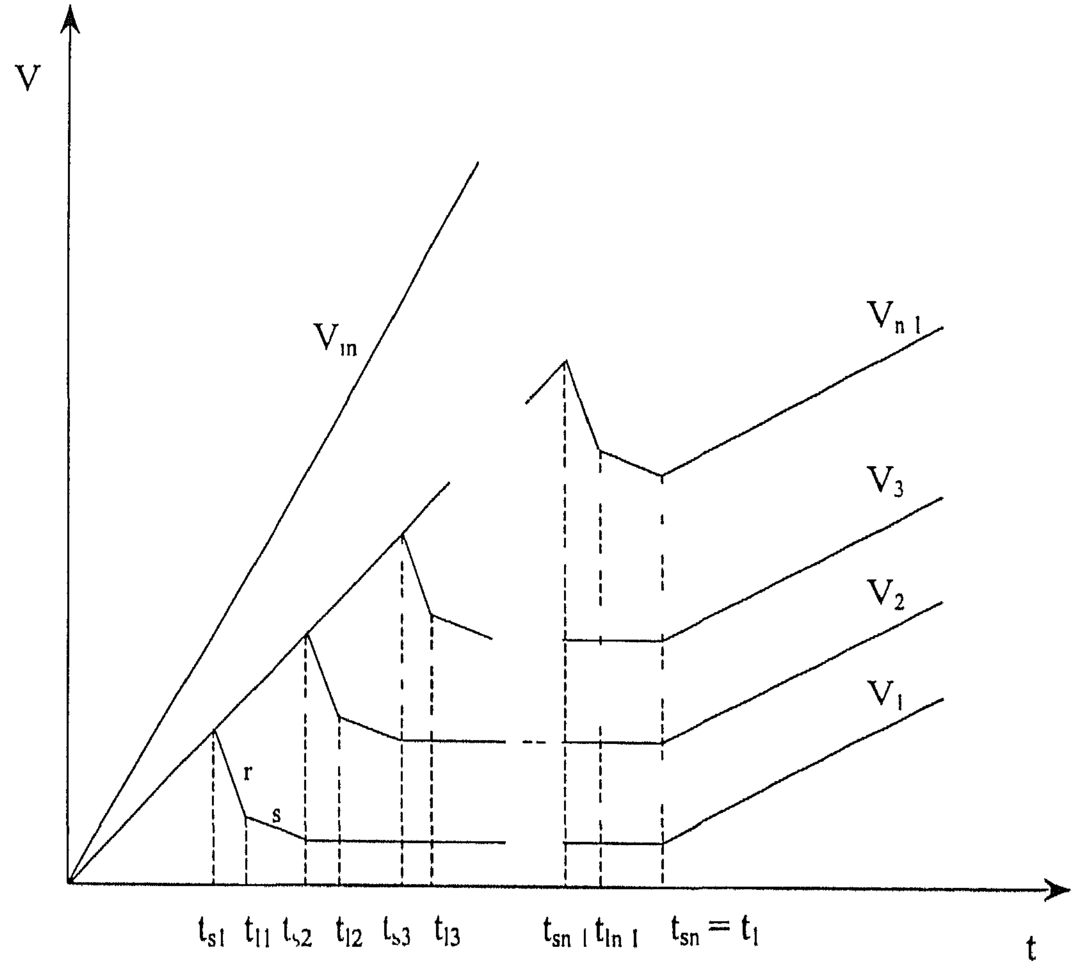


Figure 3 3 PWL of the internal node voltages till the complete transistor chain starts conduction

3 4 APPROXIMATION OF PARASITIC CAPACITANCE

Another problem involved with this two region modeling is the dependence of the parasitic capacitances on the drain source voltage which will also result in iterative expressions The reason is that the node voltages are obtained because of the charging of these parasitic capacitances and these again depend on the drain voltages To reduce this complexity and avoid sacrificing the efficiency another assumption is made for the

calculation of the capacitances in the linear region i e for the time $[t_{li}, t_{i+1}]$ The capacitance C_i at the nodes of the transistors as shown in Figure 3 1 (b) arise due to the parasitic drain substrate and the source substrate capacitances which depend on the drain source voltage when the transistor operates in the linear region The dependence is shown in Appendix I In the saturation region the value of the capacitance C_i is independent of the drain source voltage and becomes equal to $2/3(\alpha_i\ 1)C_{OX}$ (Refer Appendix I) but during the linear region it will keep on increasing and for the case of the drain source voltage becoming zero the value becomes equal to $(\alpha_i\ 1)C_{OX}$

In the linear region the drain voltages of all the transistors will be very less by the time they start operating in the linear range which will result in C_i value close to $(\alpha_i\ 1)C_{OX}$ This will increase further to reach the final value of $(\alpha_i\ 1)C_{OX}$ when the node voltages become zero So the node capacitance value has been approximated to $(\alpha_i\ 1)C_{OX}$ for the linear region This approximation leads to some loss of accuracy while allowing better efficiency because the iterative expressions reduce down to ordinary equations

3 5 CALCULATION OF STARTING POINT OF CONDUCTION

As mentioned earlier we need to calculate the average slopes r and s in order to calculate the starting point of conduction t_l For the calculation of r we calculate the value of the drain voltage of the bottom transistor for the time points t_{S1} and tl_1 as shown in Figure 3 3 The charging/discharging of the parasitic capacitances will be the same as shown in the Figure 2 1 (d) Time point t_{S1} is the time when the bottom transistor enters conduction and so will be the time at which the input ramp reaches the value of V_{TO} So, t_{s1} and the corresponding drain voltage say V_{s1} will be given by

$$t_{S1} = \frac{V_{TO}}{V_{DD}}\tau \quad \&$$

$$V_{S1} = \frac{C_{M1}}{C_{M1} + C_1} V_{TO} \tag{3 1}$$

The time point t_{l1} is the time at which the bottom transistor enters the linear region It can be calculated by applying the Kirchoff's current law equation at the node 1 of Figure 2 1 (d) and using the condition that at this time the drain source voltage of the transistor will equal its (V_{GS} V_T) A detailed derivation is given in Appendix III

$$i_1 = i_{CM1} - i_{C1} \tag{3 2}$$

$$\Rightarrow K_S\left(V_{GS} - V_{T0}\right)^{\alpha} = C_{M1}\left[\frac{dV_{l1}}{dt} - \frac{dV_{S1}}{dt}\right] - C_1\left[\frac{dV_{S1}}{dt}\right] \tag{3 3}$$

From t_{l1} the value of the drain voltage at that time say V_{l1} can be calculated and so r will be given by

$$r = (V_{s1}\ V_{l1})/(t_{l1}\ t_{s1}) \tag{3 4}$$

For calculating the value of s we need the value of drain voltage of the bottom transistor at the time points t_{l1} and t_{s2} For this time the transistor will be in the linear region and so by solving equation (3 2) with the expression of the drain current for linear region and using the condition that at time t_{s1} the transistor above the bottom transistor goes into conduction, t_{s2} can be calculated

$$\Rightarrow K_S\left(V_{GS} - V_{T0}\right)^{\alpha/2} V_{DS} = C_{M1}\left[\frac{dV_{l1}}{dt} - \frac{dV_{S1}'}{dt}\right] - C_1\left[\frac{dV_{S1}'}{dt}\right] \tag{3 5}$$

$$\& \quad V_{ln}\left(t_{S1}\right) - V_{S1}' = \theta_0 + \delta_0 V_{S1}' \tag{3 6}$$

Where V_{S1}' is the drain voltage of the bottom transistor corresponding to time t_{s1} Detailed derivation is given in Appendix III

Now, s will be given by

$$s = (V_{s1}'\ V_{l1})/(t_{s2}\ t_{l1}) \tag{3 7}$$

By generalizing the equations (3 5) and (3 6) a recursive expression for finding out the value of t_{li} can be obtained as

$$t_i = t_{S_i}\left[1 + \frac{\dfrac{C_{M_{i-1}}}{C_{M_{i-1}} + C_{i+1}}\dfrac{V_{DD}}{\tau}}{\dfrac{V_{DD}}{\tau} - r}\right] \tag{3.8}$$

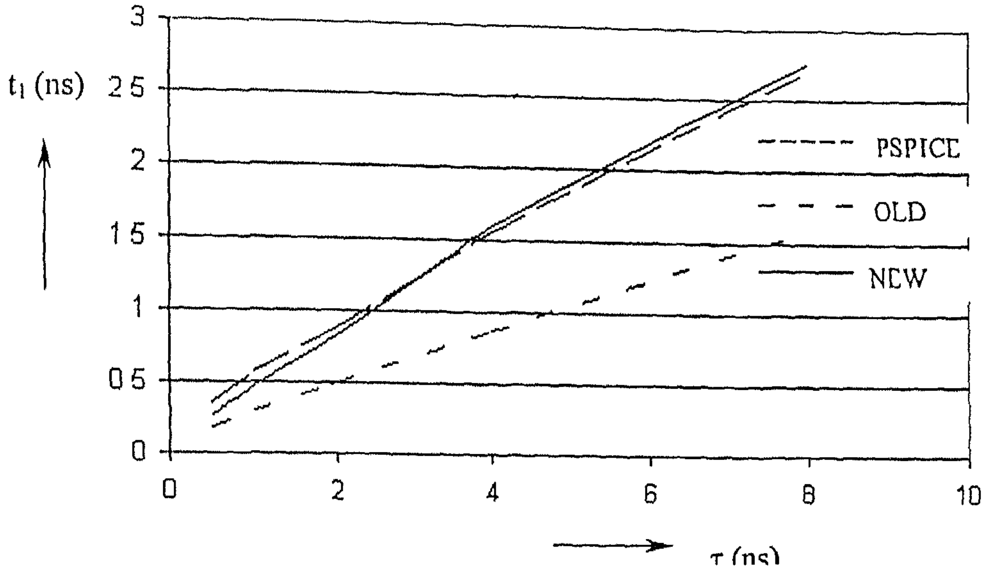
Where, t_{si} is given by

$$t_{S_i} = \frac{\left\langle \theta + (1+\delta)\left[\dfrac{C_{M_i}}{C_{M_i} + C_i}\dfrac{V_{DD}}{\tau} - r\right]t_{S_{i-1}} + (1+\delta)(r-s)t_{1,i-1}\right\rangle}{\dfrac{V_{DD}}{\tau} - (1+\delta)s} \tag{3.9}$$

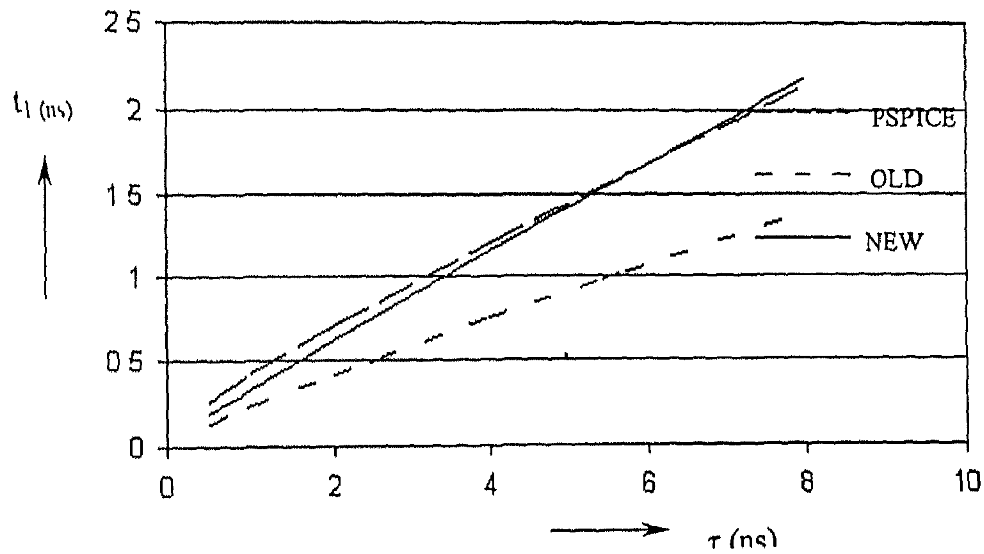
By solving these recursive expressions we can find out the value of t_1 which is nothing but t_{Sn}. The values of t_1 as calculated by this procedure and those obtained by the analysis carried out in the previous chapter have been compared with the results of PSPICE level 3 model for a transistor chain with 4 and 6 transistors and are shown in Figure 3.4 (a) and (b). The plots clearly show the increase in the accuracy of calculation of the starting point of conduction of the chain that is obtained by the new analysis. Also it can be seen that the approximations that we have taken for simplifying the equations have not introduced significant errors.

The remaining analysis has been carried out as discussed in chapter 2 for finding out t_2 and V_P and the W_{eq} has been calculated at $t = \tau$ for both the fast and the slow ramps.

The results obtained for the equivalent inverter by calculating the values of W_{eq} by using this new analysis for the starting point of conduction are far more accurate than those obtained in the previous case. A detailed discussion on the results has been presented in chapter 4.



(a)



(b)

Figure 3 4 Comparison of starting point of conduction for **(a)** n = 6 **(b)** n = 4 for different values of rise time for the input ramp (C_L=100fF L=0 5u W=8u)

Chapter 4

RESULTS AND DISCUSSIONS

4 1 RESULTS

As the accuracy of the equivalent width depends on how accurately we model the voltage at node n 1 i e the voltage V_M the gained accuracy in the calculation of t_1 and thus V_M will reflect onto accuracy of W_{eq} The improvement gained in the calculation of the starting point of conduction can be seen from the Figure 3 4 As the idea is to get the effective width of the transistor chain and thus the inverter which can be then simulated using first order models the value of the equivalent width that is obtained has been incorporated into PSPICE level 1 inverter model and the accuracy verified The increase in accuracy is evident from the Figure 4 1 where some outputs have been shown relating to different input transition times and lengths for a 4 input NAND gate In [1] the results of equivalent inverter were incorporated into ILLIADS inverter model and the outputs compared to a SPICE 3 model But since ILLIADS was not available and as it is a primitive level 1 model, the results have been verified using the PSPICE level 1 model

Since in a timing simulator, the main idea is to compute the delays the delay obtained by PSPICE level 3 model of a complete NAND gate with different number of inputs, input transition times and three different lengths has been compared with the delay obtained by incorporating the calculated effective width into a PSPICE level 1 model, and shown in Tables 4 1 4 2 and 4 3 The percentage errors calculated have also been shown and from these the increase in the accuracy obtained due to the consideration of the body effect in the calculation of the starting point of conduction can be seen

In order to verify the accuracy of this improved analysis two more complex gates and the AOI1221 have been taken and the outputs compared to that of PSPICE level 3 outputs for the same circuits

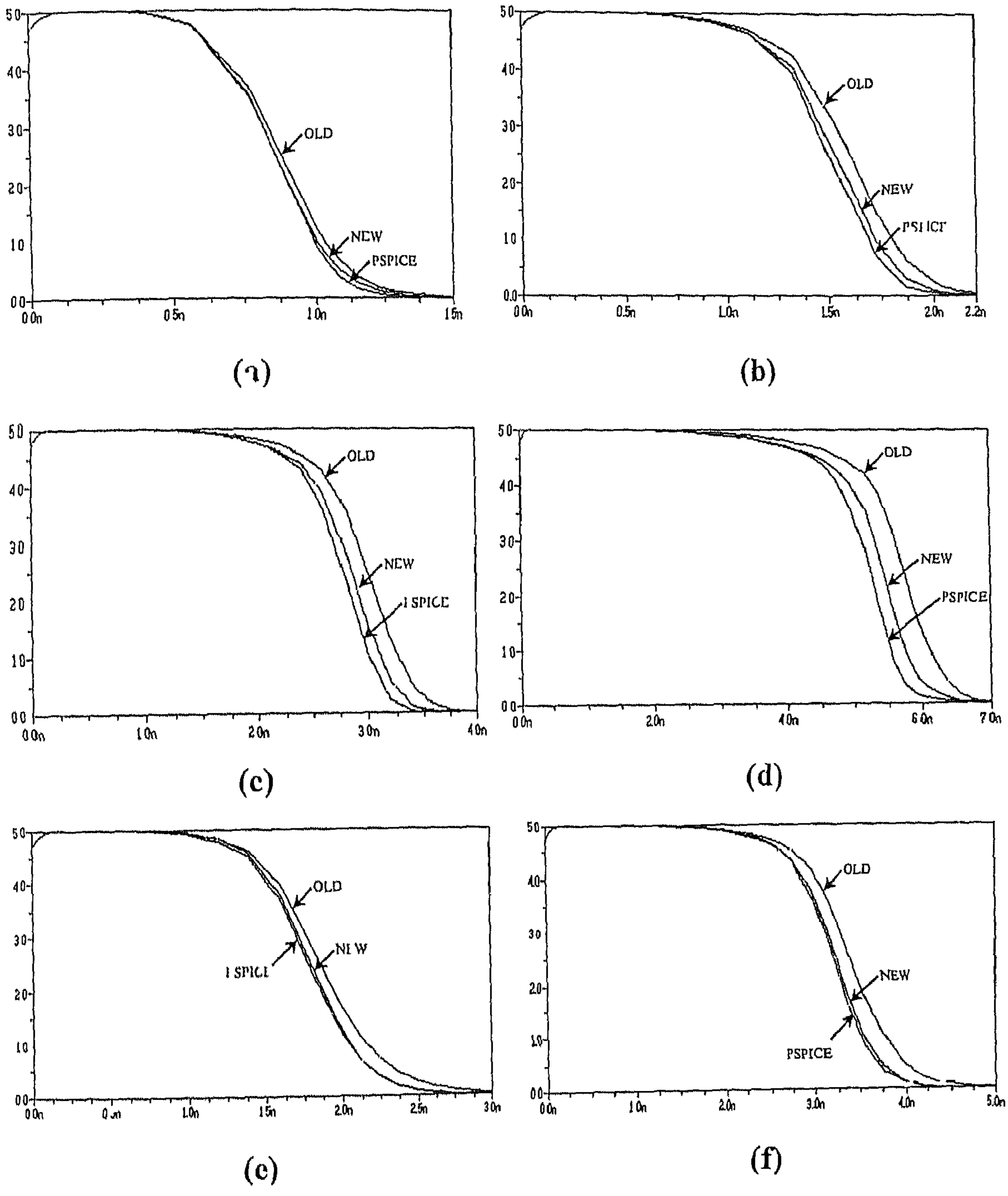


Figure 4.1 Comparison of output waveforms of PSPICE level 3 model for Gates and the equivalent inverter for L=0.5u (a) N=2 τ=1ns (b) N=2 τ=2ns (c) N=2 τ=4ns (d) N=2 τ=8ns (e) N=4, τ=2ns (f) N=4 τ=4ns

TABLE 4.1 Propagation Delays (in ns) and Percentage Errors for PSPICE level 3 model Method as proposed in [1] (Old) and the Proposed Method (New) of NAND gate with 2, 4 and 6 inputs for different input transition times and Length = 0.5u (W=8u, C_L=100fF)

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
2	0.5	0.256	0.251	1.95	0.250	2.34
2	1.0	0.347	0.370	6.63	0.350	0.87
2	2.0	0.501	0.602	20.16	0.533	6.39
2	4.0	0.774	0.991	28.04	0.851	9.95
2	8.0	1.218	1.734	42.36	1.411	15.85

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
4	0.5	0.420	0.404	3.81	0.370	11.90
4	1.0	0.504	0.504	0.00	0.501	0.60
4	2.0	0.789	0.852	7.98	0.771	2.28
4	4.0	1.192	1.380	15.77	1.220	2.35
4	8.0	1.923	2.361	22.78	2.039	6.03

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
6	0.5	0.637	0.547	14.13	0.484	24.02
6	1.0	0.739	0.709	18.00	0.638	13.67
6	2.0	1.000	1.049	4.9	0.963	3.70
6	4.0	1.497	1.686	12.63	1.452	3.01
6	8.0	2.397	2.623	9.43	2.435	1.59

TABLE 4 2 Propagation Delays (in ns) and Percentage Errors for PSPICE level 3 model Method as proposed in [1] (Old) and the Proposed Method (New) of NAND gate with 2 4 and 6 inputs for different input transition times and Length = 0 35u (W=8u C_L=100fF)

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
2	0 5	0 206	0 212	2 91	0 207	0 49
2	1 0	0 282	0 336	19 15	0 305	8 16
2	2 0	0 441	0 531	20 41	0 471	6 80
2	4 0	0 673	0 917	36 26	0 757	12 48
2	8 0	1 094	1 638	49 73	1 298	18 65

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
4	0 5	0 316	0 311	1 58	0 295	6 65
4	1 0	0 445	0 477	7 19	0 432	2 92
4	2 0	0 666	0 758	13 81	0 672	0 90
4	4 0	1 055	1 268	20 19	1 096	3 89
4	8 0	1 745	2 205	26 36	1 893	8 48

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
6	0 5	0 440	0 414	5 91	0 369	16 14
6	1 0	0 508	0 510	0 39	0 503	0 98
6	2 0	0 836	0 938	12 2	0 807	3 47
6	4 0	1 308	1 535	17 35	1 314	0 46
6	8 0	2 183	2 652	21 48	2 254	3 25

TABLE 4.3 Propagation Delays (in ns) and Percentage Errors for PSPICE level 3 model Method as proposed in [1] (Old) and the Proposed Method (New) of NAND gate with 2, 4 and 6 inputs for different input transition times and Length = 0.25u (W=8u, C_L=100fF)

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
2	0.5	0.171	0.185	8.19	0.175	2.34
2	1.0	0.241	0.294	21.99	0.263	9.13
2	2.0	0.365	0.483	32.33	0.416	13.97
2	4.0	0.586	0.858	46.42	0.701	19.62
2	8.0	0.993	1.568	57.91	1.21	21.85

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
4	0.5	0.256	0.27	5.47	0.248	3.13
4	1.0	0.385	0.421	9.35	0.381	1.04
4	2.0	0.580	0.694	19.66	0.605	4.31
4	4.0	0.947	1.179	24.50	1.012	6.86
4	8.0	1.613	2.089	29.51	1.785	10.66

N	τ	SPICE	OLD	%ERROR	NEW	%ERROR
6	0.5	0.334	0.344	0.00	0.300	10.18
6	1.0	0.482	0.502	1.04	0.469	2.70
6	2.0	0.726	0.844	16.25	0.716	1.38
6	4.0	1.186	1.425	20.15	1.204	1.52
6	8.0	2.023	2.503	23.73	2.129	9.69

Two more complex gates as shown in the Figure 4 2 and Figure 4 3 have been taken and the results have been tabulated in the Tables 4 4 and 4 5 An AOI1221 gate as shown in Figure 4 4 has also been taken and the results tabulated in Table 4 6 All these examples show the increase in the accuracy of the computation of delay when compared to the previous analysis as discussed in [1]

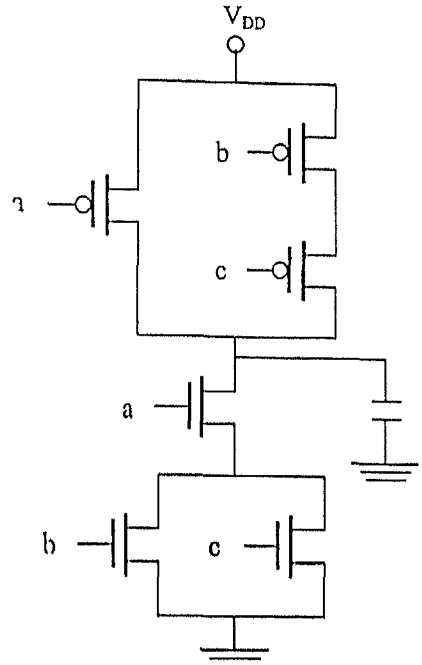


Figure 4 2 Complex Gate 1 $[a(b+c)]'$ (C_L = 100fF)

Table 4 4 Propagation Delays (in ns) and Percentage Errors for PSPICE level 3 model Equivalent NAND gate level 3 model and the Equivalent inverter level 1 model for different input transition times and Length = 0 5u

τ	PSPICE	EQ NAND	% ERROR	EQ INV	% ERROR
0 5	0 234	0 212	9 40	0 204	12 82
1 0	0 320	0 285	10 94	0 288	10 00
2 0	0 423	0 393	7 09	0 405	4 26
4 0	0 626	0 572	8 63	0 627	0 16
8 0	0 942	0 827	12 21	0 971	3 08

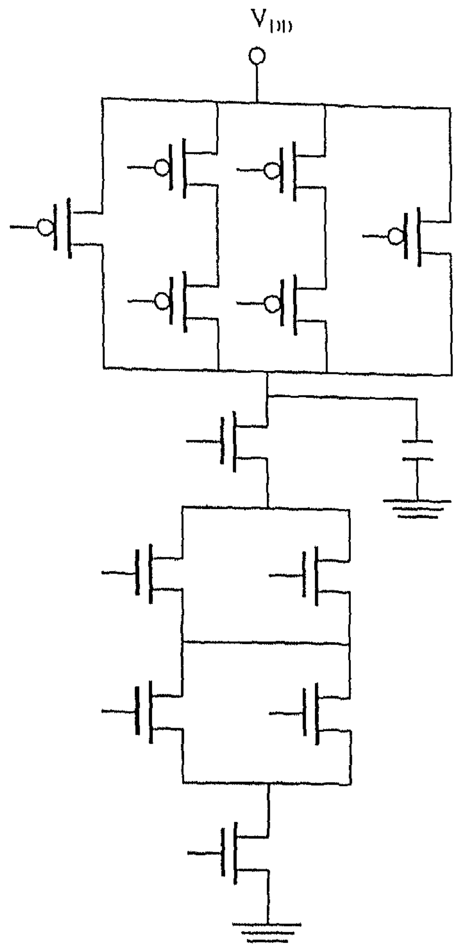


Figure 4.3 Complex Gate 2 AOI1221 circuit (C_L = 100fF)

Table 4.5 Propagation Delays (in ns) and Percentage Errors for PSPICE level 3 model Equivalent NAND gate level 3 model and the Equivalent inverter level 1 model for different input transition times and Length = 0.5u

τ	PSPICE	EQ NAND	% ERROR	EQ INV	% ERROR
0.5	0.403	0.369	8.47	0.320	20.59
1.0	0.504	0.484	3.97	0.437	13.29
2.0	0.713	0.676	5.19	0.648	9.12
4.0	1.058	0.995	5.95	1.020	3.59
8.0	1.669	1.564	6.29	1.680	0.66

4 2 CONCLUSIONS

Simulation is one of the key design validation tools that are required while designing complex integrated circuits both for checking a circuit s function as well as performance There are two methods of doing the timing analysis for checking the delay parameters of any VLSI circuits One of the methods is to analyse the voltage and currents at each and every node and do all the computation and get the result This method is the one employed by simulators such as SPICE and is the most accurate one but the problem is that for VLSI circuits the time taken by such simulators is not affordable particularly for intermediate design checks The other method is to use less accurate models to gain more efficiency in time but by compromising some of the accuracy Much research has been focussed to develop new techniques that can enhance the accuracy by using the simpler models itself there by improving both the accuracy as well as the efficiency One such technique has been presented in [1] But in the process of linearisation of the output waveforms to simplify the computations the body effect had been overlooked which has resulted in errors that could have been otherwise avoided

In this work the complete modeling mentioned in [1] has been redone with the consideration of the body effect on the threshold voltage and this has resulted in much more accurate results with only little increase in the complexity All the results shown in this chapter, clearly show the improvement gained by incorporating the body effect in the calculation of the starting point of conduction of a transistor chain while analysing complex CMOS gates

4 3 FURTHER SCOPE

It can be seen from the results that the output obtained by this new analysis is giving more accurate results for slower ramps than the faster ramps This is happening because in the PWL approximation that has been done to arrive at the simplified waveform diagram of Figure 3 3 the waveform has been shown to be always falling from the time t_{Si} to t_{Si+1} with different rates of r and s But for faster input ramps the rate of charging of the node parasitic capacitances will become greater than the drain current of

the transistor below it at the time the transistor just enters into linear region from the saturation region This will sometimes result in an increase of the node voltage instead of the decrease as has been shown So this will result in some error in the calculation of t_1 with fast input ramps This can also be seen from the Figure 3 4 where the value of t_1 matches more to that obtained by PSPICE simulations for slower ramps So if this region could be modeled more accurately then the errors can be reduced further than obtained by the current correction However this will on the other hand increase the complexity of the algorithm and thus will reduce the efficiency

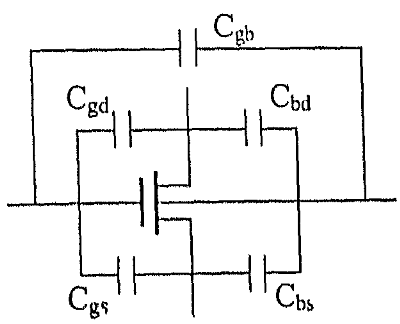
APPENDIX 1

1 Modulation of threshold voltage due to the Body effect [7]

$$V_{TN}=V_{TO}+\gamma\left[\sqrt{(V_{SB}+\phi_O)}-\sqrt{\phi_O}\right]$$

Where V_{TO} is the zero body bias threshold voltage and γ is the body effect coefficient

2 Intrinsic capacitances for a 4 terminal MOS transistor[7]



$$C_{gs}=C_{ox}\,\frac{a(1+2\eta)}{3(1+\eta)^2}$$

$$C_{bs}=(\alpha_1-1)C_{ox}\,\frac{2(1+2\eta)}{3(1+\eta)^2}=(\alpha_1-1)C_g$$

$$C_{gd}=C_{ox}\,\frac{2(\eta^2+2\eta)}{3(1+\eta)^2}$$

$$C_{bd}=(\alpha_1-1)C_{ox}\,\frac{2(\eta^2+2\eta)}{3(1+\eta)^2}=(\alpha_1-1)C_{gd}$$

$$C_{gb}=\frac{\alpha_1-1}{3\alpha_1}C_{ox}\left(\frac{1-\eta}{1+\eta}\right)^2$$

Where, $\eta= \begin{cases} 1-\dfrac{V_{DS}}{V_{DSAT}} & V_{DS}\le V_{DSAT} \\ 0 & V_{DS}> V_{DSAT} \end{cases}$

and $\alpha_1= 1+\dfrac{\gamma}{2\sqrt{\phi_0+V_{SB}}}$

3 Coupling capacitance in Figure 2 1 (C) $C_M = C_{g\,o} W_{\,1} + C_{gd} W$

Where C_{gso} and C_{gdo} are the gate source and the gate drain overlap capacitances

4 Node capacitance in Figure 2 1 (C) $C_i = C_{bd} + C_b$

APPENDIX II

1 Derivation for V_{TN} (equation 2 3)

$$V_{TN} = V_{TO} + \gamma\left[\sqrt{(V_{SB} + \phi_0)} - \sqrt{\phi_0}\right]$$

Expanding using Taylor series around $V_{SB} = 0\ 2V_{DD}$

$$V_{TN} = V_{TN}|_{V_{SB}=0\ 2V_{DD}} + V'_{TN}|_{V_{SB}=0\ 2V_{DD}}(V_{SB} - 0\ 2V_{DD})$$

$$\Rightarrow \quad V_{TN} = V_{TO} + \gamma\left(\sqrt{0\ 2V_{DD} + \phi_0} - \sqrt{\phi_0}\right) + \frac{\gamma}{2\sqrt{0\ 2V_{DD} + \phi_0}}(V_{SB} - 0\ 2V_{DD})$$

$$= \theta + \delta V_{SB}$$

where

$$\theta = V_{TO} + \gamma\left[\frac{0\ 2V_{DD} + 2\phi_0 - 2\sqrt{0\ 2V_{DD}\phi_0 + \phi_0^2}}{2\sqrt{0\ 2V_{DD} + \phi_0}}\right]$$

and $\quad \delta = \dfrac{\gamma}{2\sqrt{0\ 2V_{DD} + \phi_0}}$

2 Derivation for plateau voltage V_P (equation 2 4)

$$I_{Mu} = I_{beq}$$

$$\Rightarrow K_{Su}(V_{DD} - \theta - (1+\delta)V_p)^{\alpha} = K_{Ibeq}(V_{DD} - V_{TO})^{\alpha/2}V_p$$

Expanding L H S using Taylor series upto the second order and rearranging the terms,

$\Rightarrow$

$$V_P^2\left[\frac{\alpha(\alpha-1)}{2}(1+\delta)^2 K_{Su}(V_{DD} - \theta)^{\alpha-2}\right] - V_p\left[\alpha(1+\delta)K_{Su}(V_{DD} - \theta)^{\alpha-1} + K_{Ibeq}(V_{DD} - V_{TO})^{\alpha/2}\right] + K_{Su}(V_{DD} - \theta)^{\alpha} = 0$$

It is of the form $aV_p^2 + bV_p + c = 0$

$$\text{So, } V_p = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

3 Equation for evaluating W_{eq} (equation 2 5)

$I_{MN} = I_{Meq}$

$$\Rightarrow \frac{P_S W}{L}\left[V_i - \theta - (1+\delta)V_M\right]^{\alpha} = \frac{P_S W_l}{L}\left[V - V_{TO}\right]$$

$$\Rightarrow \quad W_{eq} = W_n\left(\frac{V - \theta - (1+\delta)V_M}{V_i - V_{TO}}\right)^{\alpha}$$

Where V_{in} V_M and W_{eq} are functions of time

4 Solution for finding t_2

$$C_L \frac{dV_0}{dt} = -K_S \left(V_{in} - \theta - (1+\delta)V_M\right)^{\alpha}$$

putting $V_M = V_1 + m(t - t_1)$ & $V_{in} = \frac{V_{DD}}{\tau}t$

$$\Rightarrow C_l \frac{dV_0}{dt} = -K_{Sn}\left\{-\theta - (1+\delta)(V_1 - mt_1) + \left[\frac{V_{DD}}{\tau} - (1+\delta)m\right]t\right\}^{\alpha}$$

$$= -K_{Sn}(a_1 + a_2 t)^{\alpha}$$

Where $a_1 = -\theta - (1+\delta)(V_1 - mt_1)$

$$a_2 = \frac{V_{DD}}{\tau} - (1+\delta)m$$

Integrating from $t = t_1$ to $t = t_2$ and using the condition that at $t = t_1$ $V_{GS} = V_T$

$$V_O(t_2) - V_O(t_1) = -\frac{K_S}{C_l}\frac{(a_1 + a_2 t_2)^{\alpha+1}}{a_2(\alpha+1)} \quad (\mathrm{a})$$

Also, at this very instant M_n enters linear region from saturation region

$\Rightarrow V_{DSn} = V_{DSATn}$

$\Rightarrow V_O(t_2) - V_M(t_2) = V_{in}(t_2) - V_M(t_2) - [\theta + \delta V_M(t_2)]$

$$\Rightarrow V_O(t_2) = \frac{V_{DD}}{\tau}t_2 - \theta - \delta\left(V_1 + m(t_2 - t_1)\right)$$

Putting in (a) and using the series expansion it will become of the form of

$$ax^3 + bx^2 + cx + d = 0$$

where

$$a = K_S a_1^{(\alpha-2)} a_2^2 \alpha(\alpha-1) / 6 C_L$$

$$b = K_S a_1^{(\alpha-1)} a_2 \alpha / 2 C_L$$

$$c = K_S a_1^{\alpha} / C_L + V_{DD}/\tau - \delta m$$

$$d = K_S a_1^{(\alpha+1)} / [a_2 C_L (\alpha+1)] - V_{DD} - 0 - \delta(V_1 - mt_1)$$

The solution will be

$$x = -\frac{b}{3a} - \frac{2^{1/3}\left(3ac - b^2\right)}{3a\left(p+q\right)^{1/3}} + \frac{\left(p+q\right)^{1/3}}{3(2^{1/3}a)}$$

where,

$$p = -2b^3 + 9abc - 27a^2d$$

and $q = \sqrt{4\left(3ac - b^2\right)^3 + p^2}$

5 Solution for finding t_{S2} (equations 2 17 & 2 18)

At $t = t_{S2}$ M_2 enters conduction

$$\Rightarrow V_{CS2} = V_{TN2}$$

$$\Rightarrow V_l\left(t_{S2}\right) - V_1\left(t_{S2}\right) = \theta_0 + \delta_0 V_1\left(t_{S2}\right)$$

$$\Rightarrow V_1\left(t_{S2}\right) = \frac{\left[\frac{V_{DD}}{\tau} t_{S2} - \theta_0\right]}{\left(1 + \delta_0\right)} \qquad \text{—(a)}$$

From equation 2 17,

$$K_S\left(V_{in}(t) - V_{TO}\right)^{\alpha} = C_{M1}\left[\frac{dV_{in}(t)}{dt} - \frac{dV_1(t)}{dt}\right] - C_1 \frac{dV_1(t)}{dt}$$

$$\Rightarrow \left(C_{M1} + C_1\right)\frac{dV_1(t)}{dt} = C_{M1}\frac{V_{DD}}{\tau} - K_S\left(V_{in}(t) - V_{TO}\right)^{\alpha}$$

Assuming $\alpha = 1$ and integrating from $t = t_{S1}$ to t_{S2}

$$\Rightarrow (C_{M1}+C_1)(V_1(t_s)-V_1(t_{s1}))=\left(C_{M1}\frac{V_{DD}}{\tau}+K_S V_{TO}\right)(t_s-t_{s1})-K_S\frac{V_{DD}}{\tau}\left(\frac{t_S^2-t_{S1}}{2}\right)$$

Using (1)

$$t_s^2\left(-\frac{K_s V_{DD}}{2\tau}\right)+t_s\left[-\left(\frac{C_{M1}+C_1}{1+\delta_0}\right)\frac{V_{DD}}{\tau}+\frac{C_{M1}V_{DD}}{\tau}+K_S V_{TO}\right]+$$

$$\left[\left(\frac{C_{M1}+C_1}{1+\delta}\right)-\frac{C_{M1}V_{DD}}{\tau}t_{S1}-K_S V_{TO}t_{S1}+K_S\frac{V_{DD}}{\tau}\frac{t^2{}_{S1}}{2}+(C_{M1}+C_1)V_1(t_{S1})\right]=0$$

Where $t_{S1}=\dfrac{V_{TO}}{V_{DD}}\tau$

And $V_1(t_{S1})=\left(\dfrac{C_{M1}}{C_{M1}+C_1}\right)V_{TO}$

It is a quadratic equation of the form $ax^2+bx+c=0$

So $t_{S2}=\dfrac{-b\pm\sqrt{b^2-4ac}}{2a}$

Putting in (1) we get $V_1(t_{S2})$

APPENDIX III

1 Solution of equation 3 1

$$t_{S1} = \frac{V_{TO}}{V_{DD}}\tau$$

$$V_{S1} = \left(\frac{C_{M1}}{C_{M1}+C_1}\right)V_{TO}$$

at $t = t_S$ $\qquad V_{GS1} = V_{IN1}$

$$\frac{V_{DD}}{\tau}t_{S2} = \theta + (1+\delta)V_{S1}^1$$

$$\Rightarrow \qquad V_{S1}^1 = \frac{\left[\frac{V_{DD}}{\tau}t_{S2} - \theta\right]}{(1+\delta)}$$

At $t = t_l$ M_1 enters linear region

$$V_{DS} = V_{GS} - V_{T1}$$

$$V_{l1} = \left(\frac{V_{DD}}{\tau}t_{l1} - V_{TO}\right) \qquad (1)$$

2 To find t_{l1} (equation 3 3)

$$K_S(V_{GS} - V_T)^\alpha = C_{M1}\left[\frac{dV_{in}}{dt} - \frac{dV_{S1}}{dt}\right] - C_1\frac{dV_{S1}}{dt}$$

Assuming $\alpha = 1$

$$\Rightarrow (C_{M1} + C_1)\frac{dV_{S1}}{dt} = C_{M1}\frac{V_{DD}}{\tau} - K_S\frac{V_{DD}}{\tau}t + K_S V_{TO}$$

$$\Rightarrow (C_{M1} + C_1)(V_{l1} - V_{S1}) = \left(C_{M1}\frac{V_{DD}}{\tau} + K_S V_{TO}\right)(t_{l2} - t_{S1}) - K_S\frac{V_{DD}}{\tau}\left(\frac{t_{l1}^2 - t_{S1}}{2}\right) \quad (2)$$

Putting (1) in (2)

$$\Rightarrow (C_{M1} + C_1)\left(\frac{V_{DD}}{\tau}t_{l1} - V_{TO} - V_{S1}\right) = \left(C_{M1}\frac{V_{DD}}{\tau} + K_S V_{TO}\right)(t_{l2} - t_{S1}) - K_S\frac{V_{DD}}{\tau}\left(\frac{t_{l1}^2 - t_{S1}^2}{2}\right)$$

Re arranging the terms, it is of the form of $ax^2+bx+c = 0$

Where

$$a = K_s \frac{V_{DD}}{2\tau}$$

$$b = (C_{M1} + C_1)\frac{V_{DD}}{\tau} - C_{M1}\frac{V_{DD}}{\tau} + K_s V_{TO}$$

$$c = -(C_{M1} + C_1)(V_{TO} + V_{S1}) + (C_{M1}\frac{V_{DD}}{\tau} + K_s V_{TO})\, t_{S1} - K_s \frac{V_{DD}}{2\tau} t_{S1}$$

$$t_{I1} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

3 To find t_{S2} (equation 3 5)

$t_{I1}<t<t_{S2}$ M_1 is in linear region

$$I_1 = I_{m1} - I_1$$

$$\Rightarrow K_l\left(\frac{V_{DD}}{\tau}t - V_{TO}\right)' V_{S1}(t) = C_{M1}\left[\frac{V_{DD}}{\tau}\right] - (C_{M1} + C_1)\frac{dV_{S1}}{dt} \quad (3)$$

We have

$$s = \frac{V_{S1}^1 - V_{I1}}{t_S - t_{I1}}$$

$$\Rightarrow \quad V_{S1}^1 = V_{I1} + s(t_{S2} - t_{I1}) \qquad (4)$$

$$V_{S1}' = \frac{\left[\frac{V_{DD}}{\tau}t_{S2} - \theta\right]}{(1+\delta)} \qquad (5)$$

Now from (3) $\quad K_l\left(\frac{V_{DD}}{\tau}t_S - V_{TO}\right)V_{S1}^1 = C_{M1}\left[\frac{V_{DD}}{\tau}\right] - s(C_{M1} + C_1) \quad (6)$

Putting $t_{S2} = \frac{\tau}{V_{DD}}\left(\theta + (1+\delta)V_{S1}^1\right)$ (from 5)

$$K_l\left(\theta - V_{TO} + (1+\delta)V_{S1}^1\right)V_{S1}^1 = \frac{C_{M1}V_{DD}}{\tau} - s(C_{M1} + C_1)$$

from (6)

$$K_l\left(\frac{V_{DD}}{\tau}t_S - V_{TO}\right)V_{S0}^1 = C_{M1}\left[\frac{V_{DD}}{\tau}\right] - s(C_{M1} + C_1)$$

using (4)

$$K_l\left(\frac{V_{DD}}{\tau}t_{S2}-V_{T0}\right)(t_{S2}-t_{l1})V^1_{S0}=C_{M1}\left[\frac{V_{DD}}{\tau}\right](t\quad -t_{l1})-\left(V^1_{S0}-V_{T0}\right)(C_{M1}+C_1)$$

using (5)

$$K_l\left(\frac{V_{DD}}{\tau}t_{S2}-V_{T0}\right)(t_S\quad -t_{l1})\frac{\left(\frac{V_{DD}t_{S2}}{\tau}-\theta\right)}{(1+\delta)}=\frac{V_{DD}}{\tau}C_{M1}(t_{S2}-t_{l1})-(C_{M1}+C_1)\left[\frac{\left(\frac{V_{DD}t_{S2}}{\tau}-\theta\right)}{(1+\delta)}-V_{T0}\right]$$

(7)

Solving (7) for t_S

It is of the form $ax^3+bx\ +cx+d=0$

$$a=\frac{K_lV^2_{DD}}{(1+\delta)\tau}$$

$$b=-\frac{K_lV_{DD}\theta}{(1+\delta)\tau}-\frac{K_lt_lV^2_{DD}}{(1+\delta)\tau^2}-\frac{K_lV_{DD}V_{T0}}{(1+\delta)\tau}$$

$$c=-\frac{C_{M1}V_{DD}}{\tau}+\frac{(C_1+C_{M1})V_{DD}}{(1+\delta)\tau}+\frac{K_l\theta t_{l1}V_{DD}}{(1+\delta)\tau}+\frac{K_lV_{T0}\theta}{(1+\delta)}+\frac{K_lt_{l1}V_{DD}V_{T0}}{(1+\delta)\tau}$$

$$d=-\frac{(C_1+C_{M1})\theta}{(1+\delta)}+\frac{C_{M1}t_{l1}V_{DD}}{\tau}-(C_1+C_{M1})V_{T0}-\frac{K_l\theta t_{l1}V_{T0}}{(1+\delta)}$$

so solution for x is

$$x=-\frac{b}{3a}-\frac{2^{1/3}\left(3ac-b^2\right)}{3a(p+q)^{1/3}}+\frac{(p+q)^{1/3}}{3(2^{1/3}a)}\qquad p=-2b^3+9abc-27a\ d$$

$$q=\sqrt{4\left(3ac-b^2\right)^3+p^2}$$

4 To find t_{l1} (equation 3 8)

At $t=t_{l1}$ M_2 enters linear region from sat

$V_{DS2}=V_{GS2}-V_{TN2}$

$$V_l\ =V_1(t_l\ )-V^1_{S1}-\theta-\delta V^1_{S1}$$

$$\text{But } V_{l2} = \left(\frac{C_{M2}}{C_{M2}+C_2}\right)\frac{V_{DD}}{\tau}t_{S2} + r(t_{l2} - t_{S2})$$

$$\Rightarrow t_{l2} = \frac{\left[\theta + (1+\delta)V_{S1}^{1}\left(\frac{C_{M2}}{C_{M2}+C_2}\frac{V_{DD}}{\tau} - r\right)t_{S2}\right]}{\left(\frac{V_{DD}^{\prime}}{\tau} - r\right)}$$

But $$\theta + (1+\delta)V_{S1}^{1} = \frac{V_{DD}}{\tau}t_{S2}$$

$$\Rightarrow \quad t_{l2} = t_{S2}\left[1 + \frac{\left(\frac{C_{M2}}{C_{M2}+C_2}\right)\frac{V_{DD}}{\tau}}{\left(\frac{V_{DD}}{\tau} - r\right)}\right]$$

$$t_l = t_s\left[1 + \frac{\left(\frac{C_M}{C_M + C}\right)\frac{V_{DD}}{\tau}}{\left(\frac{V_{DD}}{\tau} - r\right)}\right]$$

5 To find t_{S1} (equation 3 9)

at $t = t_{S2}$

$V_{GS2} - V_{TN2} = 0$

$$\frac{V_{DD}}{\tau}t_{s2} - \theta - (1+\delta)V_{S1}^{1} = 0 \quad (8)$$

Now $V_{S1}^{1} = V_{l1} + s(t_{s2} - t_{l1})$

But $$V_{l1} = \left(\frac{C_{M2}}{C_{M2}+C_2}\right)\frac{V_{DD}}{\tau}t_{S1} + r(t_{l1} - t_{S1})$$

Putting in (8)

$$t_{S2} = \frac{\left[\theta + (1+\delta)\left(\frac{C_{M2}}{C_{M2}+C_2}\frac{V_{DD}}{\tau} - r\right)t_{S1} + (r - s)(1+\delta)t_{l1}\right]}{\left(\frac{V_{DD}}{\tau} - (1+\delta)r\right)}$$

$$t_s = \frac{\left[\theta + (1+\delta)\left(\frac{C_M}{C_M + C}\frac{V_{DD}}{\tau} - i\right)t_{s-1} + (i - s)(1+\delta)t_{i-1}\right]}{\left(\frac{V_{DD}}{\tau} - (1+\delta)i\right)}$$

A 130815